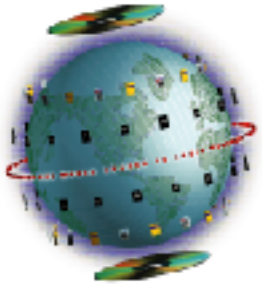
Texas Instruments

RELIABLE. LOGIC. INNOVATION.™

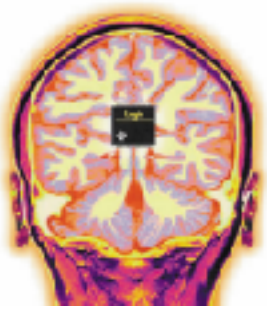
Logic Selection Guide

Second Half 2003



Service & Support

Innovation

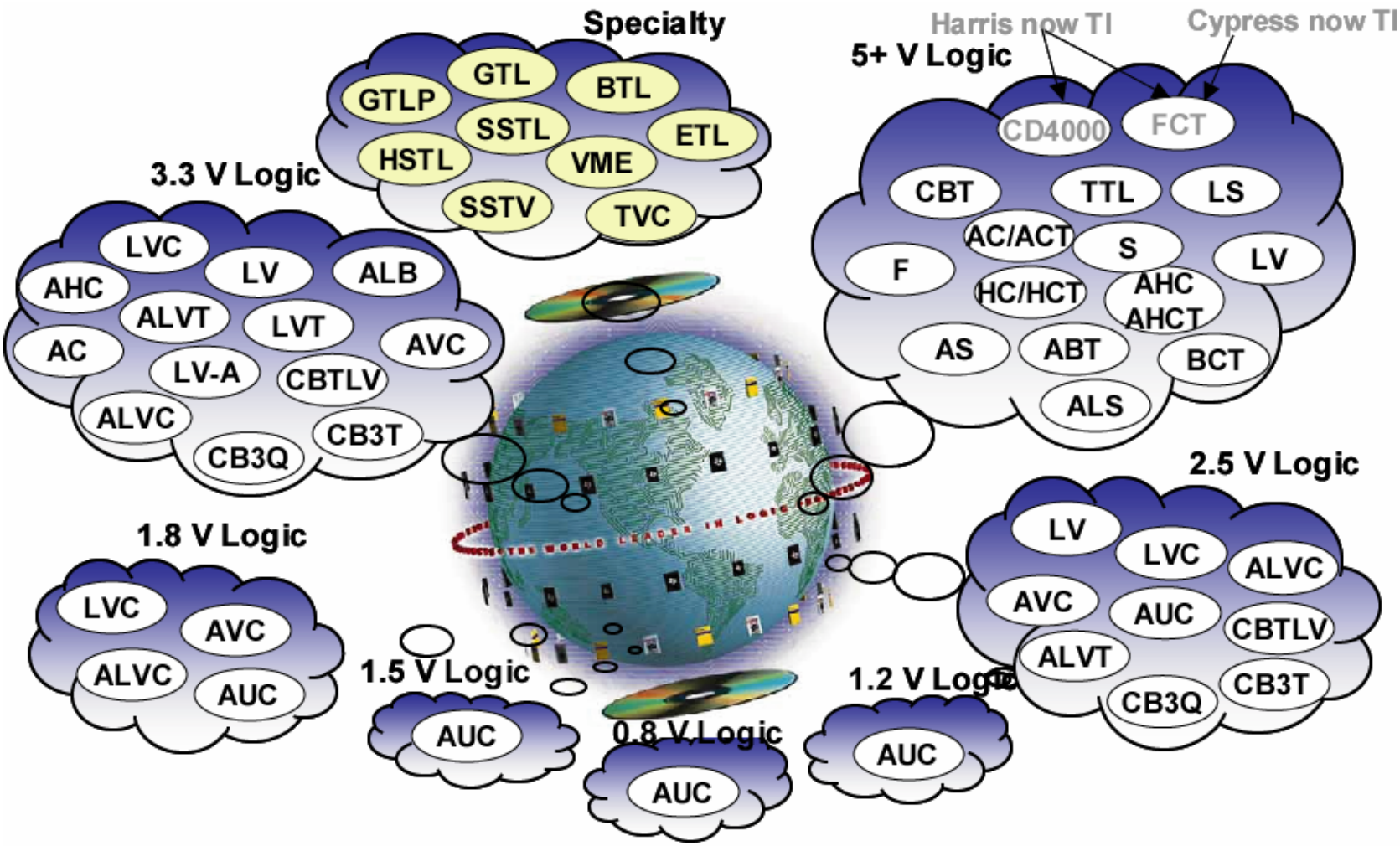


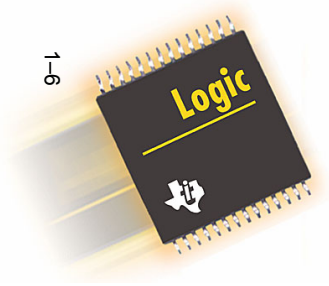
Product Breadth

Permanency

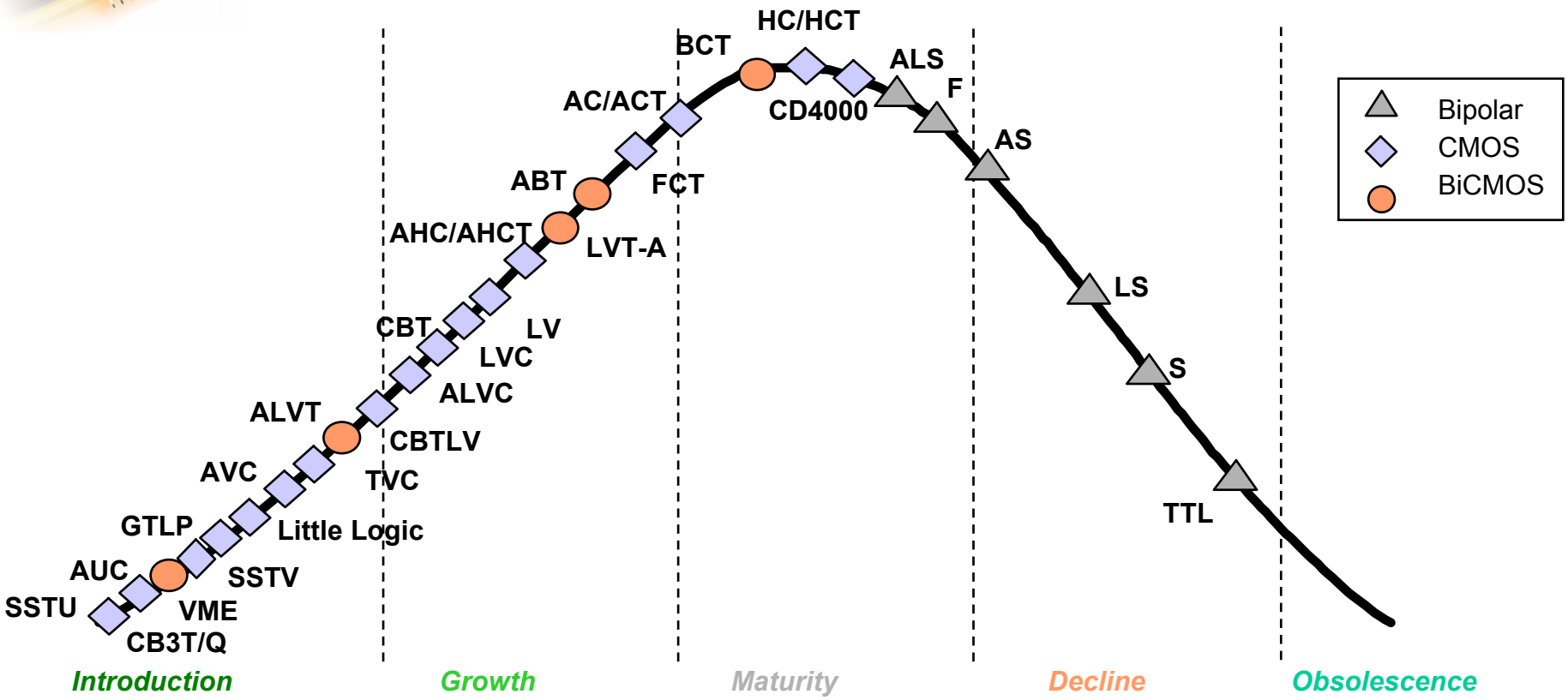
Your Logical Choice.

Welcome to the World of TI Logic





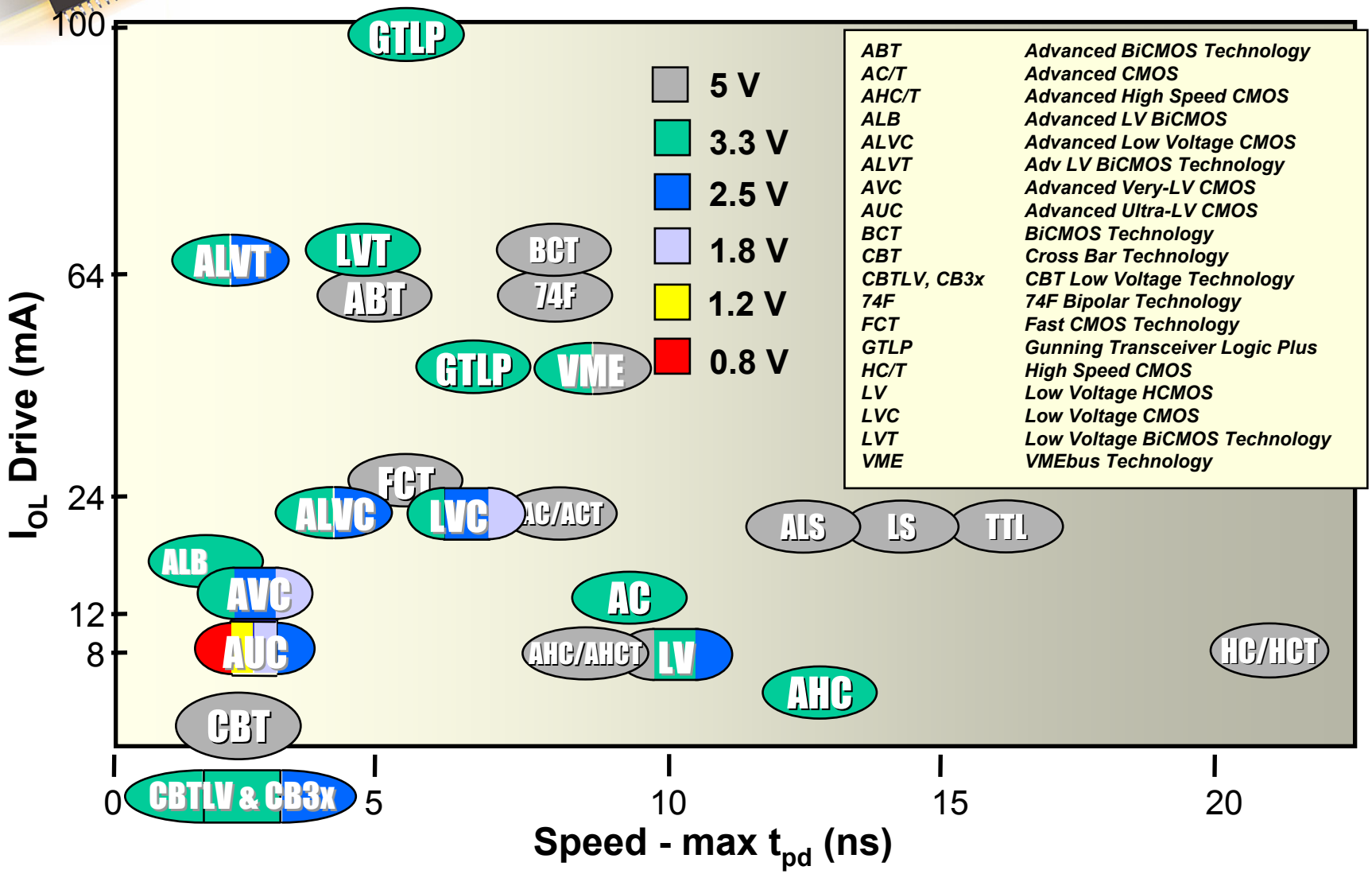
Product Life Cycle

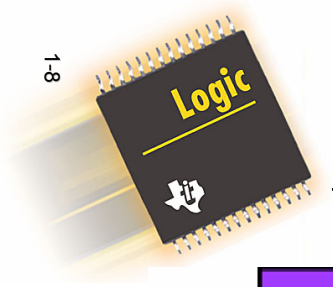


TI remains committed to be the last supplier in the older families.

Investment levels for new products are at an all-time high.

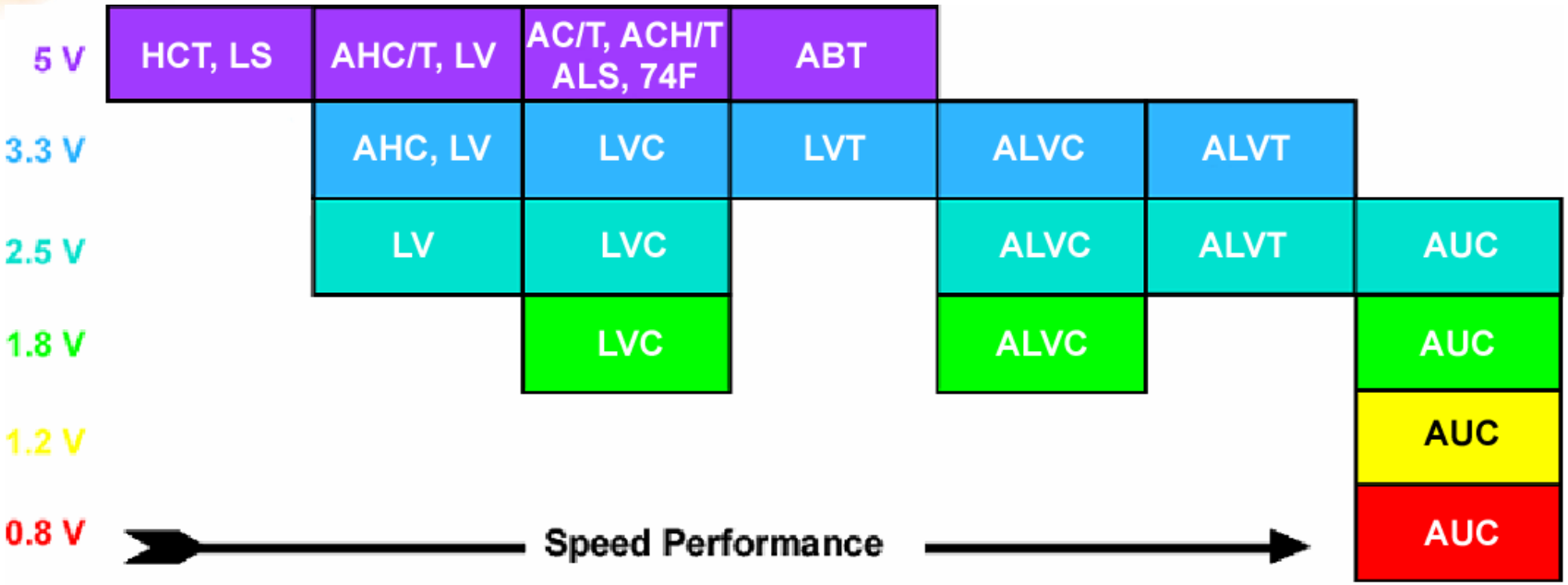
Family Performance Positioning





Low-Voltage Market

Coverage and Standardization



AHC/T
- ✓ 8.5-ns t_{pd} (5 V)
- ✓ 13.5-ns t_{pd} (3.3 V)
- ✓ –8/8 mA (5 V)
- ✓ –4/4 mA (3.3 V)
- ✓ 5-V or 3.3-V V_{CC}
- ✓ 5-V input tolerant
- ✓ 2 WW sources

LV
- ✓ 6.5-ns t_{pd} (5 V)
- ✓ 10-ns t_{pd} (3.3 V)
- ✓ –16/16 mA (5 V)
- ✓ –8/8 mA (3.3 V)
- ✓ 5-V input tolerant
- ✓ 3 WW sources
- ✓ Partial Power Down †

LVC
- ✓ 6.5-ns t_{pd}
- ✓ –24/24 mA
- ✓ Ultra-low (20 μA) standby power
- ✓ 4 WW sources
- ✓ Bus hold option
- ✓ 5-V tolerant
- ✓ Gate functions
- ✓ Partial Power Down †

LVT
- ✓ 4-ns t_{pd}
- ✓ –32/64 mA
- ✓ Low (90 μA) standby power
- ✓ 4 WW sources
- ✓ Bus hold option
- ✓ 5-V tolerant
- ✓ Hot insertion ‡

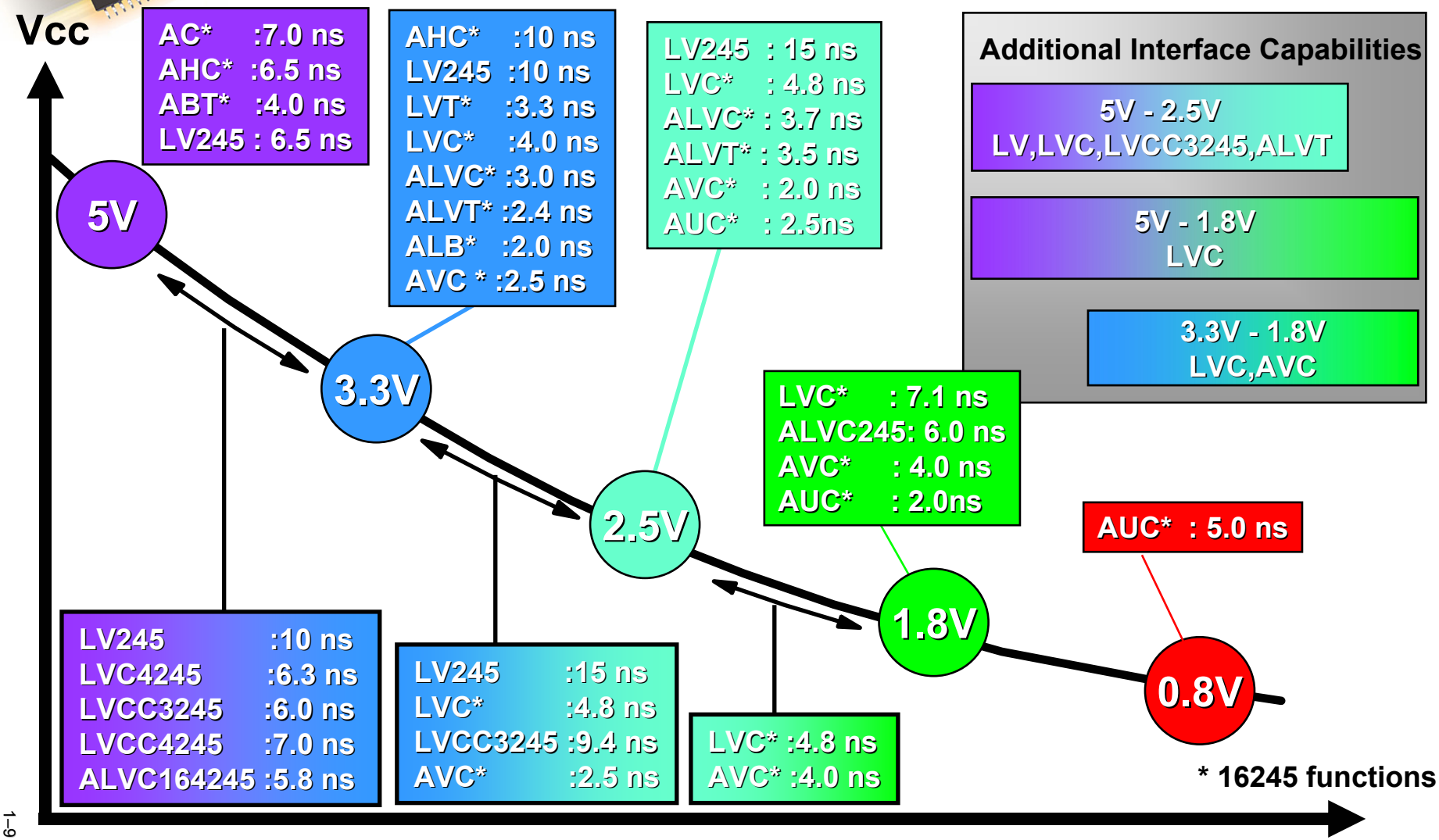
ALVC
- ✓ 3-ns t_{pd}
- ✓ –24/24 mA
- ✓ Very-low (40 μA) standby power
- ✓ 5 WW sources
- ✓ Bus hold

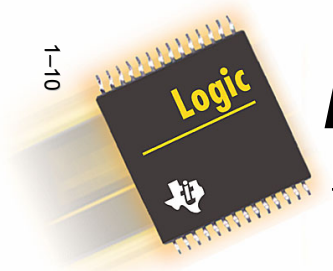
ALVT
- ✓ 2.4-ns t_{pd}
- ✓ –32/64 mA
- ✓ Low (90 μA) standby power
- ✓ 3 WW sources
- ✓ Bus hold
- ✓ 5-V tolerant
- ✓ Hot insertion ‡

AUC
- ✓ 2-ns speed
- ✓ –8/8-mA drive
- ✓ Ultra-low (10 μA) standby power
- ✓ 3 WW sources
- ✓ Bus hold option
- ✓ 3.6-V tolerant

† Partial Power Down supported by I_{off} feature
‡ Hot Insertion supported by I_{off} and Power Up 3-State features

TI Logic Supports Voltage Migration





Device Names and Package Designators

SN74 ABT H 16 2 244 A DGG R

Family
ABT/E
AC/ACT
AHC/AHCT
ALB
ALS
ALVC
ALVT
AS
AUC
AVC
BCT
CBT/LV/CB3x
CD4000
F
FB
FCT
GTL
GTLP
HC/HCT
HSTL
LS
LV-A
LVC
LVT
S
SSTL
SSTU
SSTV
SSTVF
TTL
TVC
VME

Standard Prefix
Military (54)
Commercial (74)

Special Feature
Blank = no special features
A, B, C = Configurable V_{CC}
D = Level Shifting Diode
H = Bus Hold
K = Undershoot Clamp
R = Damping Resistor on Inputs/Outputs
S = Schottky Clamping Diodes
Z = Power Up 3 State

Bit Width
Blank = Gates, MSI, and Octals
1G = Single Gate
2G = Dual Gate
3G = Triple Gate
8 = Octal IEEE 1149 (JTAG)
16 = Widebus™ (16,18, and 20)
18 = Widebus IEEE 1149.1 (JTAG)
32 = Widebus+™ (32 and 36 bit)

Options
Blank = No Options
2 = Series Damping Resistor on Outputs
3 = Level Shifter
4 = Level Shifter
25 = 25Ω Line Driver

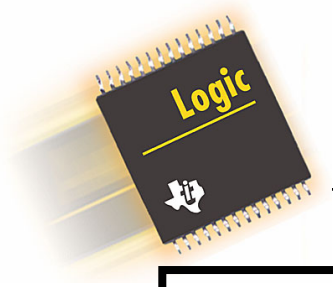
Function
00
174
244

Device Revision
Blank = No Revision
Letter Designator A-Z

Package Type
D,DW = SOIC
DB,DL = SSOP
DBB,DGV = TVSOP
DCT,DCU = TSSOP
DBV, DCK = SOT
DGG,PW = TSSOP
FK = LCCC
FN = PLCC
GB = CPGA
GKE,GKF = LFBGA
GQL = VFBGA
HFP,HS,HT,HV = CQFP
J,JT = CDIP
N,NP,NT = PDIP
PAG,PAH,PCA,PCB,PM, PN, PZ = TQFP
PH,PQ,RC = QFP
RGY,RGQ = QFN
W,WA,WD = CFP
YEA,YEP,YZA,YZP = DSBGA†

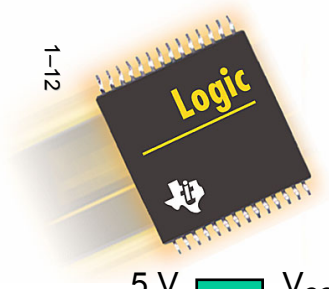
Tape & Reel
R = 3000
T = 250

† DSBGA is the JEDEC reference for wafer chip scale package (WCSP).



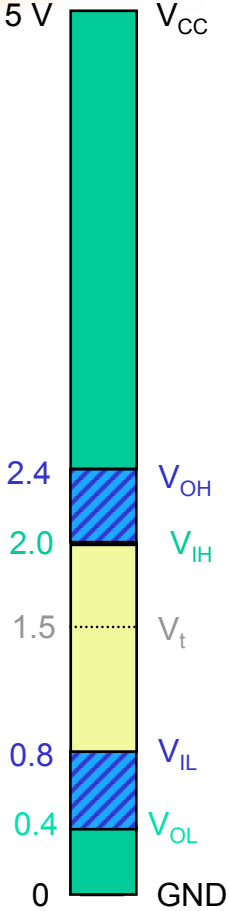
Logic Vendor Partnerships

Performance Range	TI	Philips	(Renesas) Hitachi	IDT	Toshiba	FSC	On
5 V high	ABT	ABT	ABT		ABT	ABT-C	
5 V low	AHC	AHC			VHC	VHC	VHC
3 V high	CBT-LV			CBT-LV			
3 V high	ALVT	ALVT					
3 V high / medium	ALVC	ALVC	ALVC	ALVC	VCX	VCX	VCX
3 V medium	LVT	LVT	LVT			LVT	
3 V medium	LVC	LVC	LVC	LVC	LCX	LCX	LCX
3 V low	LV-A	LV	LV-A		LVQ	LVQ	LVQ
3 V low						LVX	LVX
2.5 V high	AVC	AVC					
1.8 V high	AUC	AUC		AUC			



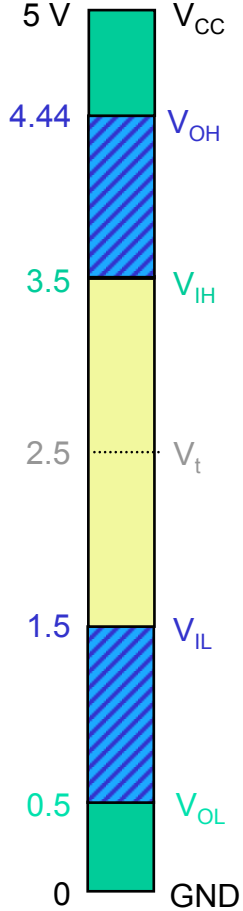
IC Basics

Comparison of Switching Standards



5-V TTL

Standard TTL: ABT, AHCT, HCT, ACT, Bipolar

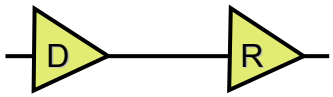


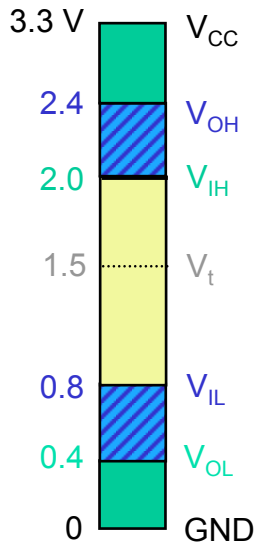
5-V CMOS

Rail-to-Rail 5 V HC, AHC, AC, LV-A

Is V_{OH} higher than V_{IH}?

Is V_{OL} less than V_{IL}?



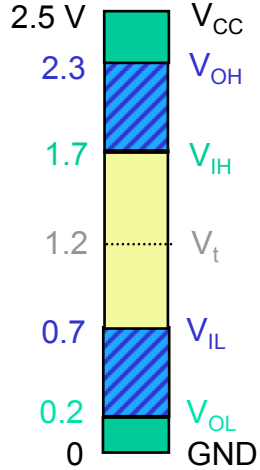


3.3-V LVTTL

LVT, LVC, ALVC, LV-A, ALVT

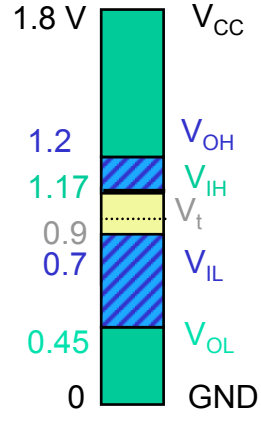
D \ R	5TTL	5CMOS	3LVTTL	2.5CMOS	1.8CMOS
5TTL	Yes	No	Yes *	Yes*	Yes*
5 CMOS	Yes	Yes	Yes*	Yes*	Yes*
3 LVTTL	Yes	No	Yes	Yes*	Yes*
2.5 CMOS	Yes	No	Yes	Yes	Yes*
1.8 CMOS	No	No	No	No	Yes

* Requires V_{IH} Tolerance



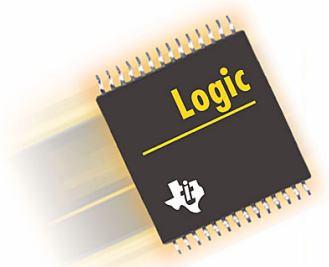
2.5-V CMOS

AUC, AVC, ALVC, LVC, ALVT



1.8-V CMOS

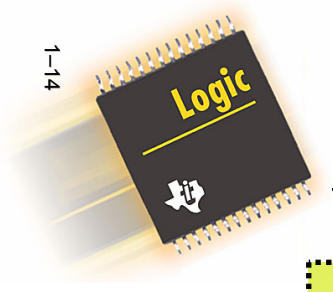
AUC, AVC, ALVC, LVC



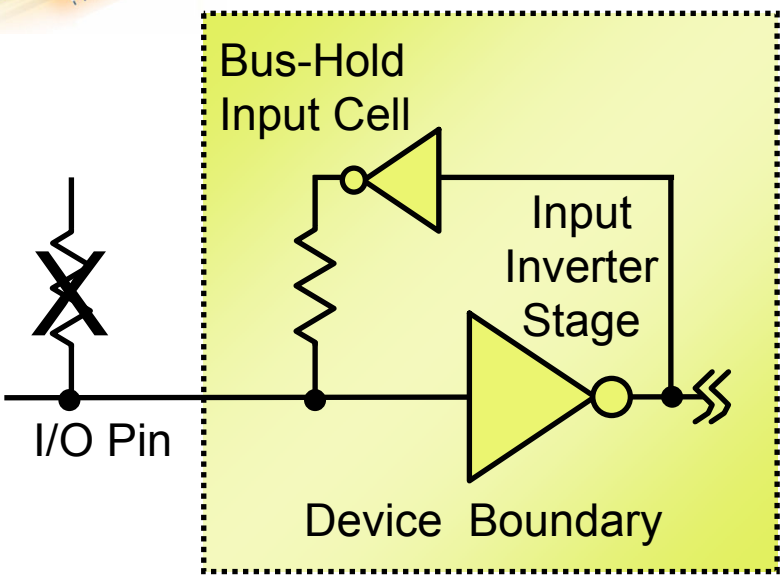
Logic Feature List †

- **Bus Hold – ABT, ALVC, ALVT, AVC, AUC, FCT, GTL, GTLP, LVC, LVT, VME**
  - Bus-hold circuitry in selected logic families helps solve the problem of floating inputs and eliminates the need for pull-up or pull-down resistors by holding the last known state of the input. See $I_{I(HOLD)}$ or I_{BHL}, I_{BHH}, I_{BHLO}, and I_{BHHO} on data sheet.
- **Series Damping Resistors – ABT, ALVC, ALVT, F, GTLP, LVC, LVT, VME**
  - Series damping resistors limit signal overshoot and undershoot by providing better impedance matching and line termination without the need for external resistors.
- **Partial Power Down (Level 1 Isolation - Ioff) – ABT, ALVT, AVC, AUC, CBTLV, CBT-C, GTL, GTLP LV-A, LVC, LVT, VME**
  - I_{OFF} circuitry prevents the device from being damaged during hot insertion. See I_{OFF} specifications on data sheet.
- **Hot Insertion (Level 2 Isolation – Ioff and Power-up 3-state) – ABT, ALVT, GTLP, LVCZ, LVT, VME**
  - Power-up 3-state ensures valid output levels during power up and valid Z on the outputs during power down. See I_{OZPU}, I_{OZPD}.
- **Live Insertion (Level 3 Isolation – Ioff, Power-up 3-state, and BIAS V_{CC}) – GTLP, FB, CBT, CBTLV, VME**
  - Precharges I/O capacitance, preventing glitching of active data.
- **Mixed-Voltage-Tolerant I/Os and Level Shifting – AVC, ALVC, ALVT, AUC, GTL, GTLP, LV-A, LVC, LVT**
  - Systems use mixed supply voltages and TLL or CMOS levels in many designs. Most advanced-logic families allow mixed-signal interfacing and provide level-shifting functions for certain mixed-voltage applications.
- **JTAG – ABT, ACT, BCT, LVT**

(†selected functions)



Bus-Hold Input

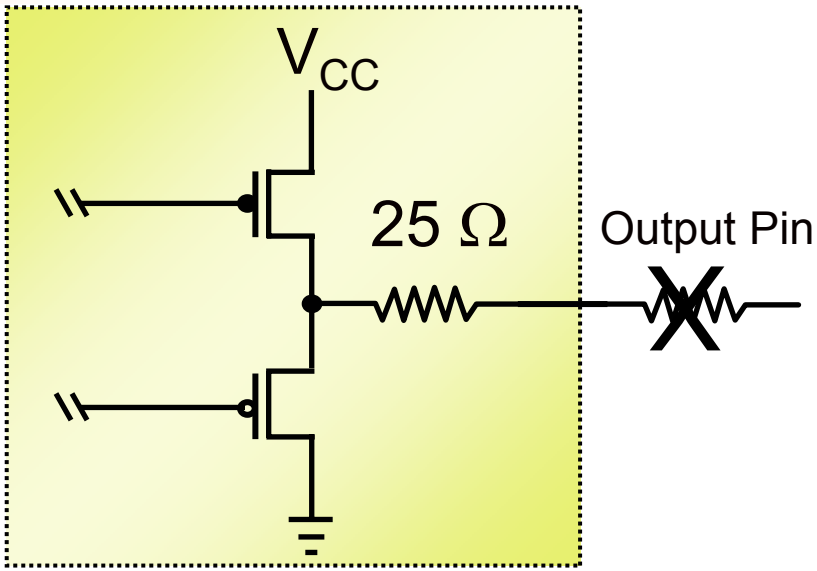


Bus-hold input cell replaces pullup resistor

- Holds the last known state of the input – avoids floating inputs
- $I_{i(HOLD)}$ or I_{BHL}, and I_{BHH} specifies min holding current
- Bus-hold current does NOT load down the driving output significantly at valid logic levels.
- Eliminates the need for external resistors on unused or floating input/output pins
- The “H” in the device name indicates bus hold.
- Negligible increase in systems power consumption.

Families Providing Bus-Hold Options
ABT, ALVC, ALVT, AVC, AUC, FCT, GTL, GTLP, LVC, LVT, VME

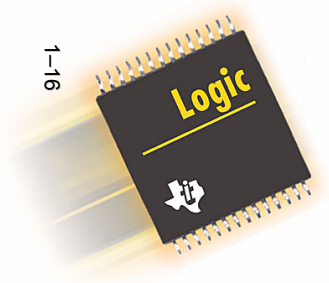
Series Damping Resistors



Damping resistors replace external series resistors

- Improves signal integrity
- Provides better impedance matching and line termination
- Eliminates the need for external series resistors
- Extra “2” or “R” in device name indicates damping resistor option
  - R: I/O pins (LVCHR16245)
  - 2: Output pins (LVC162244)

Families Providing Damping Resistor Options
ABT, ALVC, ALVT, F, GTLP, LVC, LVT, VME



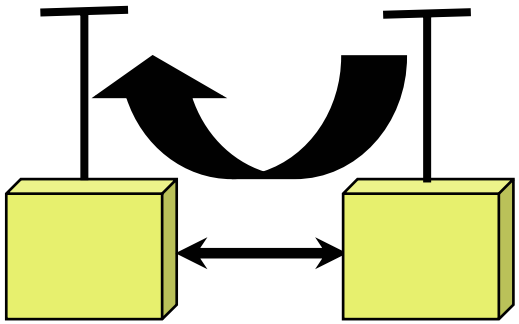
Partial Power Down

Live Insertion, Level 1

System Function Capability

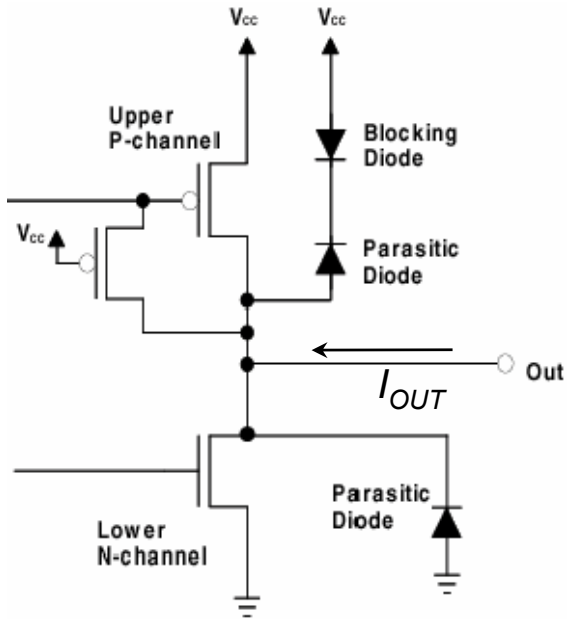
V_{CC} = 0 V

V_{CC} = 5 V



bus

- Prevents unexpected device behavior during power up or power down
- Prevents signals from sourcing current through parasitic diodes
- Allows for power down of partial circuits within a system
- I_{off} spec is required for partial power down operations



When V_{CC} = 0, I_{OUT} = 0 for $V_{OUT} > V_{CC}$.

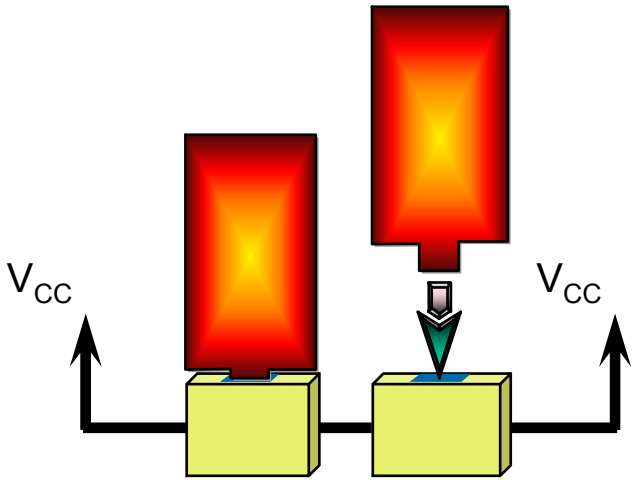
Families Supporting Partial Power Down (I_{off})

ABT, ALVT, AVC, AUC, CBTLV, CBT-C, GTL, GTLP LV-A, LVC, LVT, VME

Hot Insertion

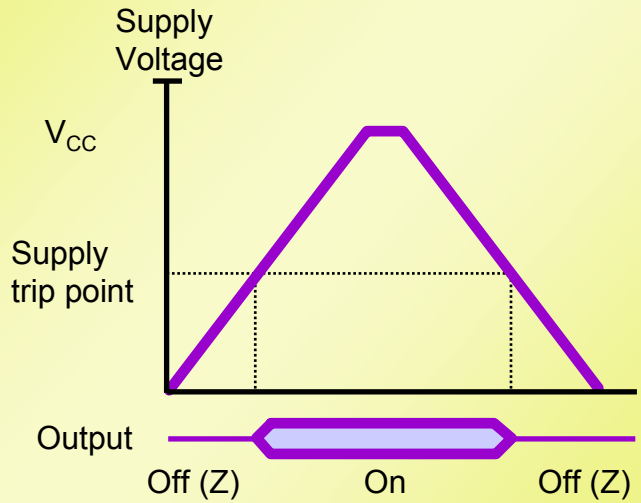
Live Insertion, Level 2

System Function/Capability



- Prevents unwanted turn-on of output before V_{CC} trip point
- Prevents bus to be loaded down upon power up of device
- Allows for hot insertion
- I_{off} and PU3S specs are required for Hot Insertion

Example
Circuit Implementation
PU3S Circuit

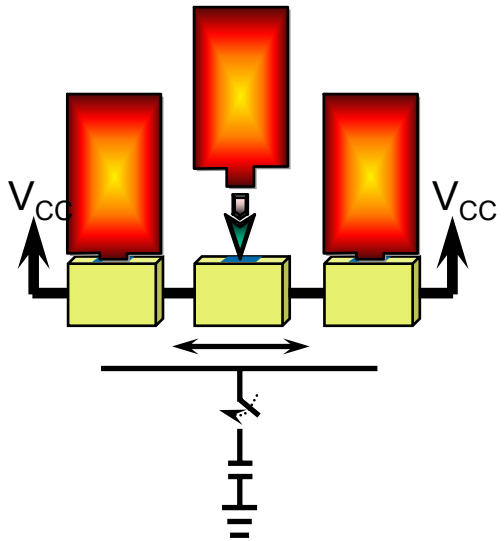


Families Supporting Hot Insertion (I_{off} and Power-up 3-state)
ABT, ALVT, GTLP, LVCZ, LVT, VME

Live Insertion

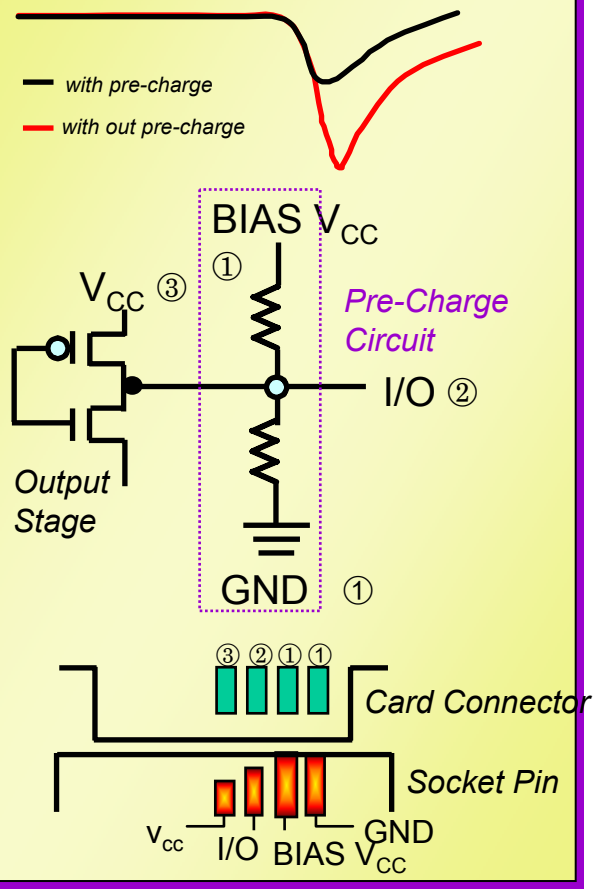
Live Insertion, Level 3

System Function/Capability



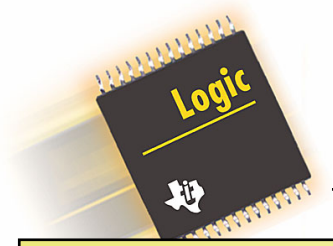
- Prevents unwanted glitches at the I/O
- Allows for live insertion
- I_{off}, PU3S, and BIAS V_{CC} required for Live Insertion
- Staggered pins required pre-charge functionality

Circuit Implementation
Pre-Charge Circuit



Families Supporting Live Insertion (I_{off}, Power-up 3-state, and BIAS V_{CC})

GTLP, FB, CBT, CBTLV, VME



Mixed-Voltage Interfacing

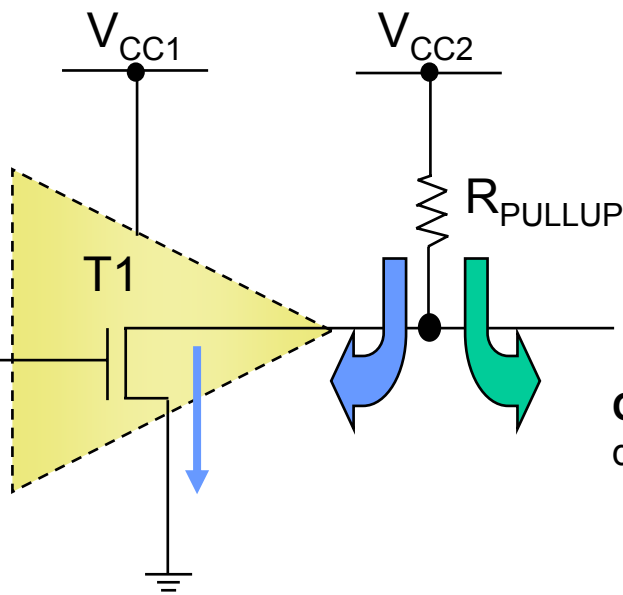
Open-Drain Outputs 05/06/07 Functions

Functions Available

05 - S, LS, ALS, AC, HC, AHC, LV, LVC
06 - TTL, LS, LV, LVC, LVC1G/3G, AUC1G
07 - TTL, LS, LV, LVC, LVC1G/3G, AUC1G

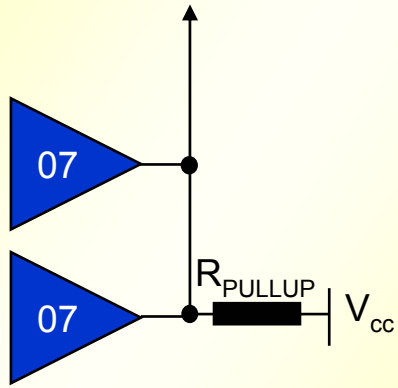
NOTE: Over voltage tolerance is required to support UP translation.

Required **Input** level depends on V_{CC1}



Output level depends on V_{CC2}

Also Possible
Wired-Function Technique

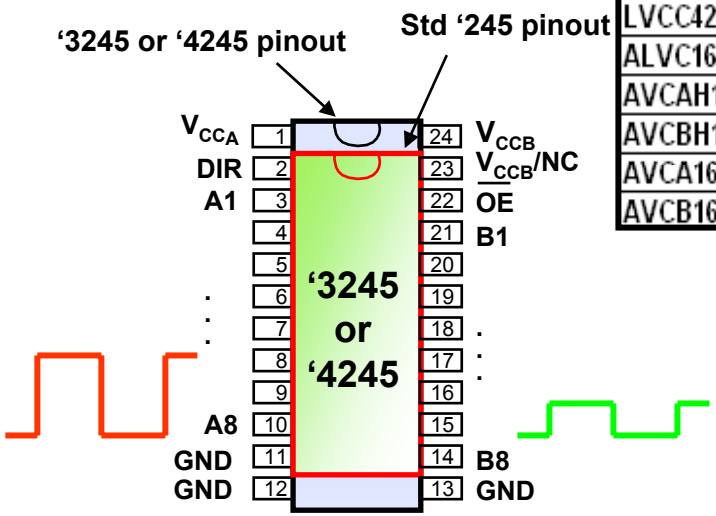


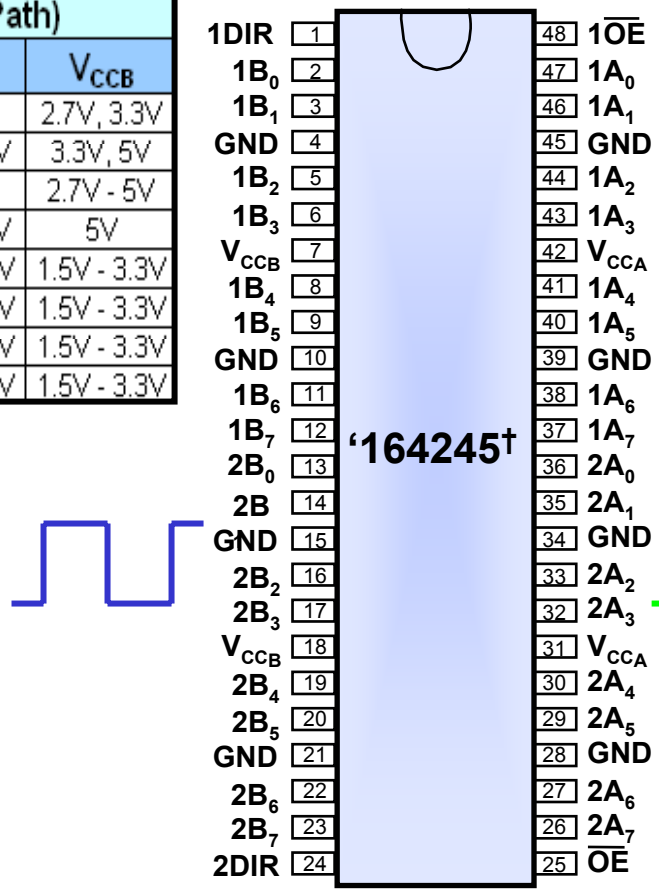
Phantom links on output side can reduce component count.

Supply Voltage Vcc1	LV05A/06A/07A		LVC06A/07A		LVC1G07/2G07/3G07		Pullup resistor may be connected to	Level conversion range
	Vi Level	Speed	Vi Level	Speed	Vi Level	Speed		
1.8 V	NA	NA	1.8 V Levels	1- 3.5 ns	1.8 V Levels	2.4 - 8.3 ns	1.8V, 2.5V, 3.3V and 5V	1.8 V ⇨ 1.8V - 5.5V
2.5 V	2.5 V Levels	6.6 - 10.4 ns	2.5 V Levels	1 - 2.8 ns	2.5 V Levels	1 - 5.5 ns	1.8V, 2.5V, 3.3V and 5V	2.5 V ⇨ 1.8V - 5.5V
3.3 V	3.3 V Levels	5 - 7.1 ns	3.3 V Levels	1 - 2.9 ns	3.3 V Levels	1.5 - 4.2 ns	1.8V, 2.5V, 3.3V and 5V	3.3 V ⇨ 1.8V - 5.5V
5 V	5 V Levels	3.4 - 5.5 ns	5 V Levels	1 - 2.6 ns	5 V Levels	1 - 3.5 ns	1.8V, 2.5V, 3.3V and 5V	5 V ⇨ 1.8V - 5.5V

Special "Dual-Supply" Level Shifters

Split Rail (Bidirctional Path)		
Device	V_{CCA}	V_{CCB}
LVC4245A	5V	2.7V, 3.3V
LVCC3245A	2.5V, 3.3V	3.3V, 5V
LVCC4245A	5V	2.7V - 5V
ALVC164245	2.7V, 3.3V	5V
AVCAH164245	1.5V - 3.3V	1.5V - 3.3V
AVCBH164245	1.5V - 3.3V	1.5V - 3.3V
AVCA164245	1.5V - 3.3V	1.5V - 3.3V
AVCB164245	1.5V - 3.3V	1.5V - 3.3V





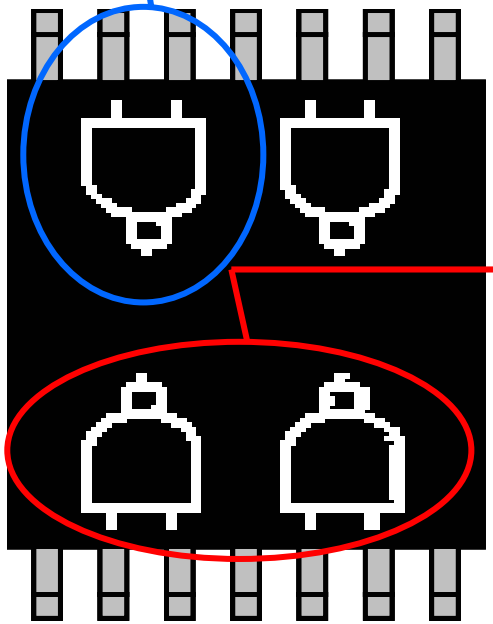
† equivalent to standard 16245 pinout.

** This solution is compatible with a 3.3-V-only system. Devices can be replaced later with 3.3-V parts with minimal PCB redesign*

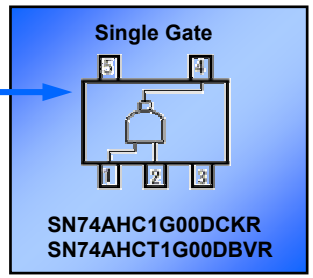
What Is Little Logic?

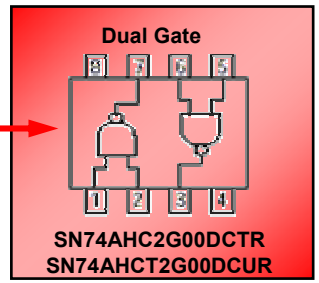
Single Gate/Dual Gate/Triple Gate

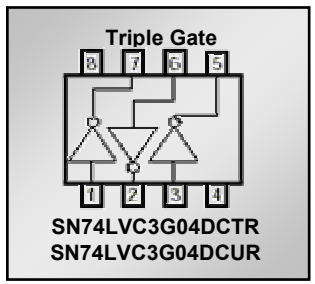
The Principle



Example







Naming

SN74 LVC 1G xx YEP R

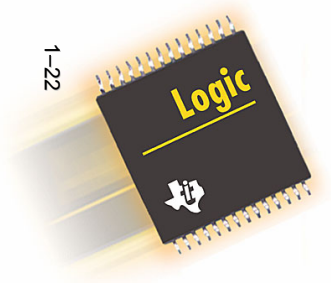
Tape & Reel
R = 3000 piece
T = 250 piece

Package Type
YEA = NanoStar™ (170u)
YEP = NanoStar™ (230u)
YZA = NanoFree™ (170u)
YZP = NanoFree™ (230u)
DCK = SC-70
DBV = SOT-23
DCU = US-8
DCT = SM-8

Logic Function
xx

Gate Count
1G - Single Gate
2G - Dual Gate
3G - Triple Gate

Product Family
AHC, AHCT, LVC, CBT, AUC

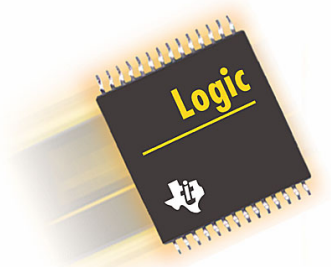


Little Logic

TI Portfolio

- Provides wide range of operating voltages (0.8V to 5.5V)
- World's first 1.8V optimized logic family (AUC) NEW!
- World's smallest Logic package solution (NanoStar™/NanoFree™)

Family	Operating Voltage	Optimized Voltage	Prop Delay$_{typ}$	Output Drive	V_i Tolerant	I_{off}
AUC	0.8-2.7V	1.8V	2.0ns	8mA	3.6V	Yes
LVC	1.65-5.5V	3.3V	3.5ns	24mA	5.5V	Yes
AHC	2.0-5.5V	5.0V	5.0ns	8mA	5.5V	No
CBT	4.5-5.5V	5.0V	0.25ns	n/a	5.5V	n/a
CBTD	4.5-5.5V	5.0V	0.25ns	n/a	5.5V	n/a
CBTLV	2.3-3.6V	3.3V	0.25ns	n/a	3.6V	Yes

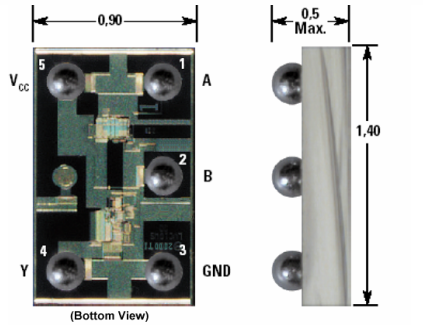


NanoStar™/NanoFree™ Package

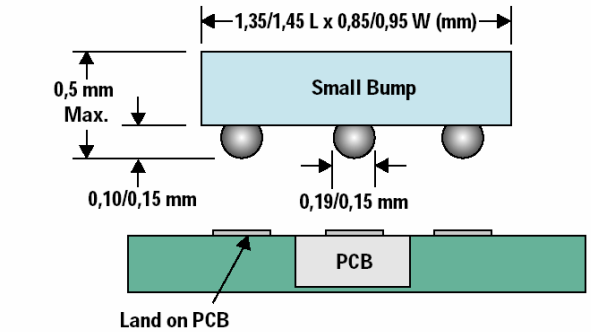
The World's Smallest Logic Package

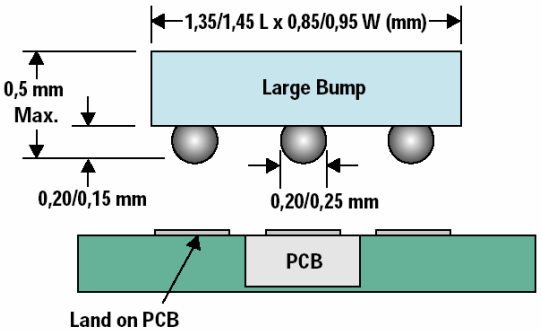
- Offered in SnPb (NanoStar) and Pb-free (NanoFree)
- Two solder bump sizes available (170u and 230u diameter)
- Bump locations facilitate device probing and rework
- 0.5-mm height meets aggressive LCD design requirements
- 70% smaller than industry standard SC-70 (DCK)
- 13% smaller than any other logic package available
- Improved thermal and electrical characteristics
- Targeted for space constrained, portable applications: Cellular, DVD/CD ROMs, DVC, Digital Watch, DSC, MD/MP3/CD players, notebook computers, PC cards and PDA's

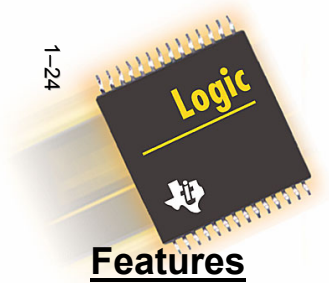
Package Designators
YEA = SnPb Small Bump
YZA = Pb Free Small Bump
YEP = SnPb Large Bump
YZP = Pb Free Large Bump



Package Area Configuration (0,5-mm Ball Pitch)







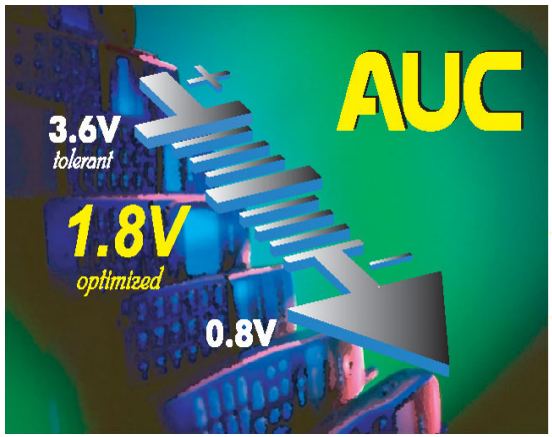
AUC

The World's First 1.8-V Logic

NEW FAMILY

Features

- 1.8-V Optimized Performance
- V_{CC} Specified at 2.5 V, 1.8 V, 1.2 V
- 0.8 V Typical
- Balanced Drive
- 3.6-V I/O Tolerance
- Bus Hold Option
- I_{OFF} Spec for Partial Power Down
- ESD Protection
- Low Noise
- Alternate -Source Agreements



Advanced Packaging

NanoStar™ YEA, YEP
NanoFree™ YZA, YZP
SOT 23 - DBV (Microgate)
SC-70 - DCK (PicoGate)
TSSOP - PW & DGG
TVSOP - DGV
LFBGA - GKE, GKF
VFBGA - ZKE, ZKF
VFBGA - GQL
VFBGA - ZQL
QFN - RGY

Device	V_{CC}	Drive	$T_{PD(MAX)}$
SN74AUC1G00	1.8 V	–8/8 mA	2.5 ns
SN74AUC16244	1.8 V	–8/8 mA	2.0 ns

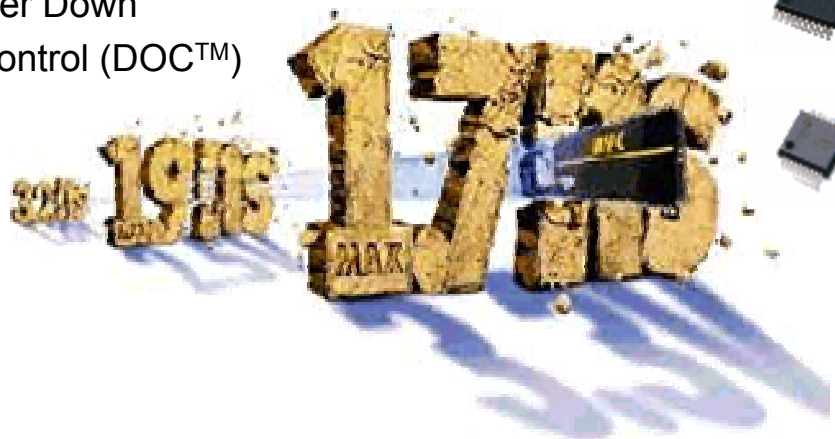
Alternate Source: Philips, IDT

AVC

Features

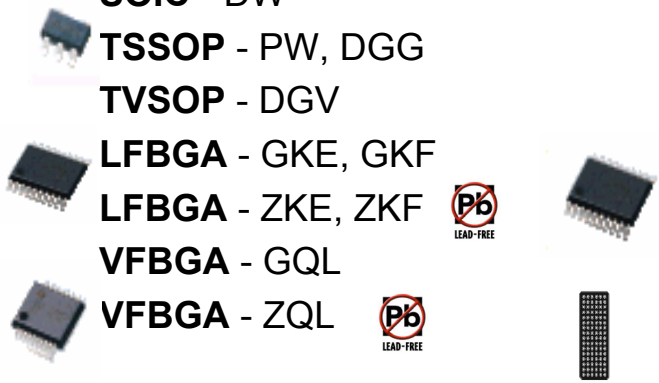
V_{CC} Specified at 3.3 V, 2.5 V, 1.8 V

- 3.3-V I/O Tolerance
- Sub-2.0-ns max T_{pd} at 2.5 V
- Bus Hold Option
- I_{OFF} for Partial Power Down
- Dynamic Output Control (DOC™) Circuit



Advanced Packaging

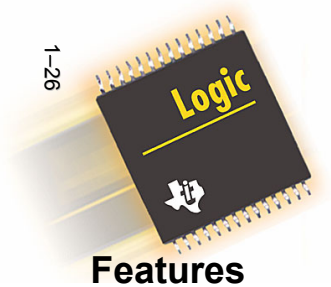
SOIC - DW
TSSOP - PW, DGG
TVSOP - DGV
LFBGA - GKE, GKF
LFBGA - ZKE, ZKF
VFBGA - GQL
VFBGA - ZQL



Device	V_{CC}	Drive	$T_{PD(MAX)}$
SN74AVC16244	3.3 V	–12/12 mA (static)	1.7 ns
	2.5 V	–8/8 mA (static)	1.9 ns
	1.8 V	–4/4 mA (static)	3.2 ns

Alternate Source: Philips

DOC is a trademark of Texas Instruments.



ALVC Family

Features

- V_{CC} Specified at 3.3 V, 2.5 V, and 1.8 V
- Balanced Drive
- Bus-Hold Option
- Drive Capability –6/12 mA at 2.5 V
- Low Noise
- Damping Resistor Options
- ESD Protection

Advanced Packaging

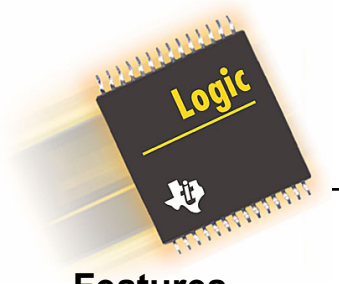
SOIC - D and DW
SSOP - DB and DL
TSSOP - PW and DGG
TVSOP - DGV

LFBGA - GKE, GKF
LFBGA - ZKE, ZKF
VFBGA - GQL
VFBGA – ZQL

Device	V_{CC}	Drive	$T_{PD(MAX)}$
SN74ALVCH244	3.3 V	–24/24 mA	2.8 ns
SN74ALVCH16244	3.3 V	–24/24 mA	3.0 ns

Literature
ALVC Low-Voltage CMOS Logic Data Book
Lit # SCED006

Alternate Source
ALVC: Philips, Hitachi, IDT
VCX: Fairchild, ON, Toshiba



LVC Family

Features

- V_{CC} Specified at 3.3 V, 2.5 V, and 1.8 V
- Balanced Drive
- 5-V I/O Tolerance
- Bus-Hold Option
- Series Damping Resistor Option
- I_{OFF} Spec for Partial Power Down
- ESD Protection
- LVCZ has Power-Up 3-State for Hot Insertion

Advanced Packaging

NanoStar™ - YEA, YEP

NanoFree™ - YZA, YZP

SOT 23 - DBV (Microgate)

SC-70 - DCK (PicoGate)

SOIC - D and DW

SSOP - DB and DL

TSSOP - PW and DGG

TVSOP - DGV

LFBGA - GKE, GKF

LFBGA - ZKE, ZKF

VFBGA - GQL

VFBGA – ZQL

NEW

QFN - RGY

Device	V_{CC}	Drive	$T_{PD(MAX)}$
SN74LVCH244	3.3 V	–24/24 mA	5.9 ns
SN74LVCH16244	3.3 V	–24/24 mA	4.1 ns

Literature

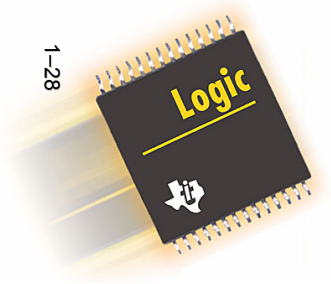
LVC Low-Voltage CMOS Logic Data Book — Lit # SCBD152

LVC Designers Guide Application Report — Lit # SDZAE16

Alternate Source

LVC: Philips, Hitachi, IDT

LCX: Fairchild, Motorola, Toshiba



LV-A Family

Features

- V_{CC} Specified at 5.0 V, 3.3 V, 2.5 V
- 5-V I/O Tolerance
- Balanced Drive
- I_{OFF} Spec for Partial Power Down
- ESD Protection
- Low Noise

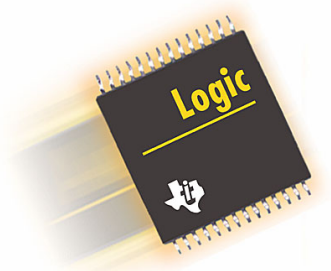
Advanced Packaging

SOIC - D, DW
SOP - NS
SSOP - DB
TSSOP - PW, DGG
TVSOP - DGV
NEW
QFN - RGY, RGQ

Device	V_{CC}	Drive	$T_{PD(MAX)}$
SN74LV244A	5.0 V	–16/16 mA	6.5 ns
	3.3 V	–8/8 mA	10.0 ns

Literature
LV Low-Voltage CMOS Logic Data Book
Lit # SCBD152

Alternate Source
LV: Philips, Hitachi
LVQ: Fairchild, ON, Toshiba
LVX: Fairchild, ON



LVT Family

Features

- V_{CC} Specified at 3.3 V
- High-Drive Output – up to 64 mA
- 5-V I/O Tolerance
- Bus Hold Option
- Partial Power Down (I_{OFF})
- Power - Up 3-State (I_{OZPU} ,I_{OZPD})
- Hot Insertion (I_{OFF} and PU3S)
- Low Noise
- Damping Resistor Options

Advanced Packaging

SOIC - DW

SSOP - DB and DL

TSSOP - PW and DGG

TVSOP - DGV

LFBGA - GKE and GKF

LFBGA - ZKE and ZKF

VFBGA - GQL

VFBGA - ZQL

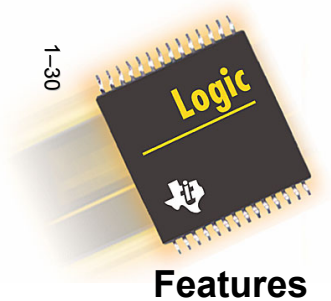
Device	V_{CC}	Drive	$T_{PD(MAX)}$
SN74LVTH244	3.3 V	–32/64 mA	3.5 ns
SN74LVTH16244	3.3 V	–32/64 mA	3.2 ns

Literature

LVT Low-Voltage Technology Data Book
Lit # SCBD154
LVT-to-LVTH Conversion Application Report
On the Internet

Alternate Source

LVT: Philips, Hitachi,
Fairchild*, ON*
** Similar Device, No Second-Source Agreement*



ALVT Family

Features

- V_{CC} Specified at 3.3 V and 2.5 V
- High-Drive Output – up to 64 mA
- 5-V I/O Tolerance
- Power-Up 3-State (I_{OZPU} ,I_{OZPD})
- Partial Power Down (I_{OFF})
- Hot Insertion (I_{OFF} and PU3S)
- Bus Hold

Advanced Packaging

SSOP - DL
TSSOP - DGG

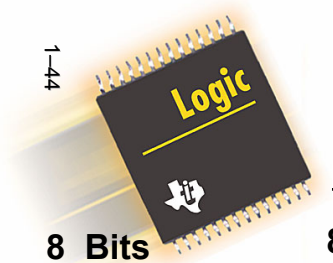
TVSOP - DGV

LFBGA - GKE and GKF
LFBGA - GKE and GKF Pb LEAD-FREE
VFBGA - GQL
VFBGA - ZQL Pb LEAD-FREE

Device	V_{CC}	Drive	$T_{PD(MAX)}$
SN74ALVTH16244	3.3 V	–32/64 mA	2.4 ns
	2.5 V	–8/24 mA	3.0 ns

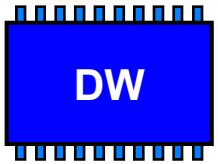
Literature
ALVT Low-Voltage Technology Data Book
Lit # SCED003

Second Source
ALVT: Philips



Packaging Options

8 Bits



20-Pin SOIC
Area = 137 mm²
Ht. = 2.65 mm
LP = 1.27 mm

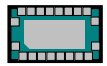
8 Bits

20-Pin SSOP
Area = 62 mm²
Ht. = 2.0 mm
LP = 0.65 mm

8 Bits

20-Pin TSSOP
Area = 46 mm²
Ht. = 1.1 mm
LP = 0.65 mm

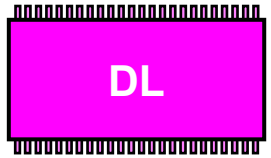
8 Bits



RGY, RGQ

20-Pin QFN
Area = 15.75mm²
Ht. = 0.9 mm
LP = 0.5mm

16/18 Bits
Widebus™



48-Pin SSOP
Area = 171 mm²
Ht. = 2.74 mm
LP = 0.635 mm

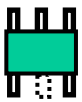
16/18 Bits
Shrink Widebus™

48-Pin TSSOP
Area = 108 mm²
Ht. = 1.1 mm
LP = 0.5 mm

16/18 Bits
Widebus™

48-Pin TVSOP
Area = 63 mm²
Ht. = 1.2 mm
LP = 0.4 mm

Little Logic Packaging - 1G/2G/3G (magnified for detail)



DBV

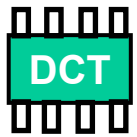
5/6-Pin SOT-23
Area = 8.12 mm²
Ht. = 1.2 mm
LP = 0.95 mm

DCK

5/6-Pin SC-70
Area = 4.2 mm²
Ht. = 1.0 mm
LP = 0.65 mm

YEA/YEP
YZA/YZP

5/6-Pin DSBGA†
NanoStar™/NanoFree™
Area = 1.26 mm²
Ht. = 0.5 mm
LP = 0.5 mm



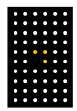
8-Pin SOT
Area = 8.26 mm²
Ht. = 1.3 mm
LP = 0.65 mm

8-Pin SOT
Area = 4.6 mm²
Ht. = 0.9 mm
LP = 0.5 mm

YEA/YEP
YZA/YZP

8-Pin DSBGA†
NanoStar™/NanoFree™
Area = 1.71 mm²
Ht. = 0.5 mm
LP = 0.5 mm

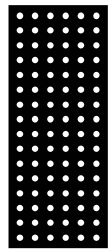
16/18 Bits
MicroStar Jr.™



GQL
ZQL

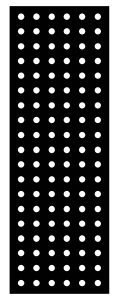
56-Ball VFBGA
Area = 31.5 mm²
Ht. = 1.0 mm
LP = 0.65 mm

32 Bits
MicroStar™



GKE
ZKE

96-Ball LFBGA
Area = 74.25 mm²
Ht. = 1.3 mm
LP = 0.8 mm



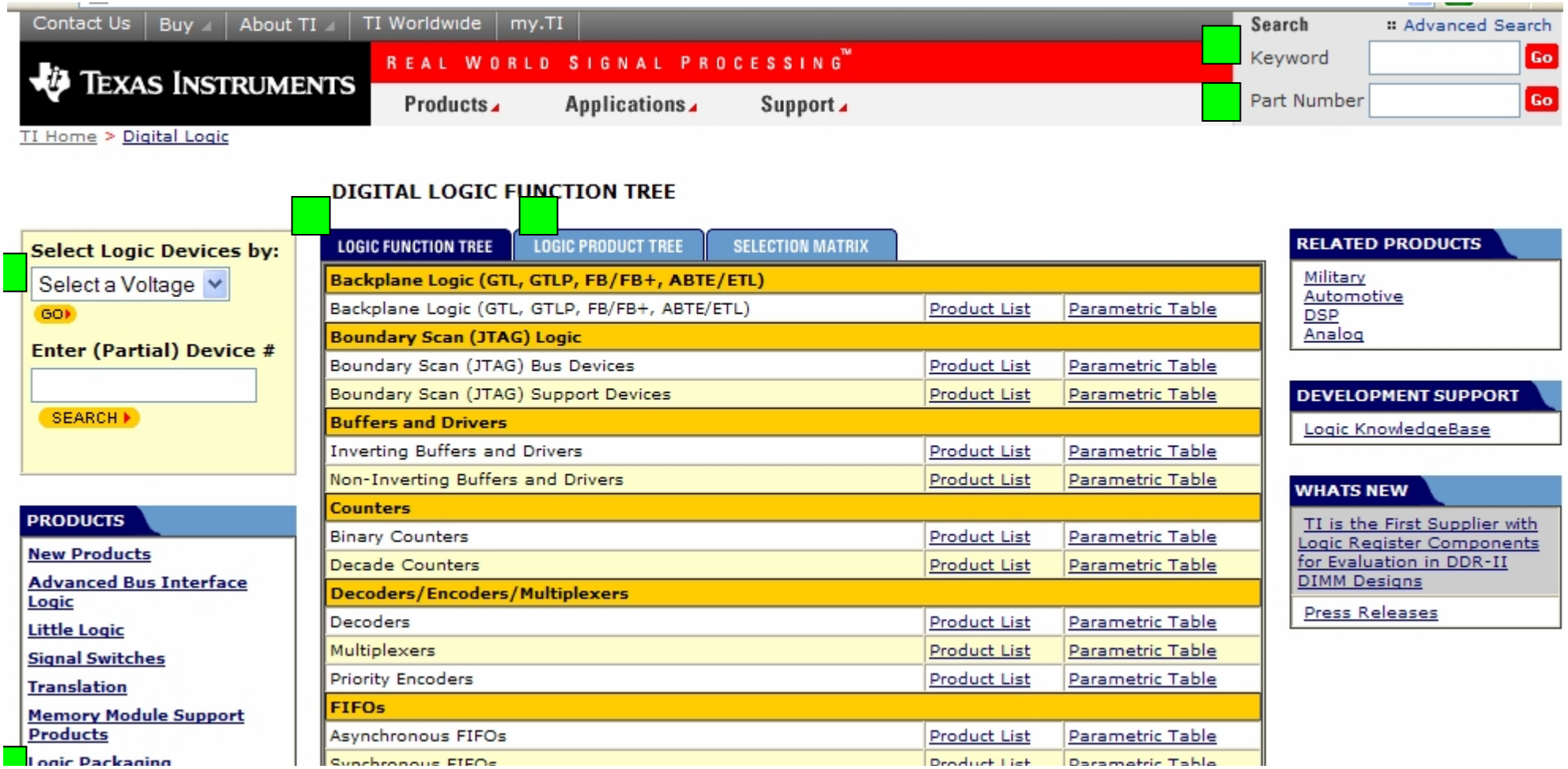
GKF
ZKF

114-Ball LFBGA
Area = 88 mm²
Ht. = 1.3 mm
LP = 0.8 mm

 † DSBGA is the JEDEC reference for wafer chip scale package (WCSP).

Web user reference to Searching logic.ti.com

Searching: If you know the…	Look here…
1. logic **Keyword** or **Phrase**	1. http://logic.ti.com – Search box (top right corner of page)
2. full or partial **Part Number**	2. http://logic.ti.com – Search box (top right corner of page)
3. **Voltage Node**	3. http://logic.ti.com – "Select a Voltage" (top left box)
4. Logic **Function** (ie: buffer, gate, register)	4. http://logic.ti.com – "Logic Function Tree" tab (top center)
5. Logic **Family** or **Product** (ie: ABT, LVT, SSTV)	5. http://logic.ti.com – "Logic Product Tree" tab (top center)
6. **Top Side Marking** on Package	6. http://logic.ti.com – "Logic Packaging" "Part Marking Lookup"



Web user reference to Navigating logic.ti.com

For technical support please contact the Product Information Center at (972) 644-5580

Support Tools & Other Web Features	Look here…
1. New Product & Package Releases	1. http://logic.ti.com – "Products" container "New Products"
2. Logic Packaging Information (advanced packaging, tape & reel, lead-free, etc.)	2. http://logic.ti.com – "Products" container "Logic Packaging"
3. Cross References (find TI equivalent devices to other logic manufacturers)	3. http://logic.ti.com – "About Logic" container "Cross Reference Search" or http://www.ti.com/logiccrossref
4. Logic eNews (sent out once a month)	4. http://logic.ti.com – "About Logic" container "Logic Newsletter"
5. Product Change Notifications (PCN's)	5. http://logic.ti.com – "About Logic" container "PCN Service"
6. Application Notes (sorted by Logic family)	6. http://logic.ti.com – "Technical Documents" container "App Notes"
7. Data Sheets (for a specific Logic part number)	7. http://logic.ti.com – Part Number Search Product Folder "Datasheet"
8. Data Sheets (across a certain Logic family)	8. http://logic.ti.com – "Technical Documents" container "Data Sheets"
9. IBIS Models (sorted by Logic family)	9. http://logic.ti.com – "Technical Documents" container "IBIS Models"
10. SPICE Models (sorted by Logic family)	10. http://logic.ti.com – "Technical Documents " container "Spice Models"
11. Logic Literature (electronic download or online order form)	11. http://logic.ti.com – "Technical Documents" container "Logic Literature"
12. Logic Samples (for a specific Logic part number)	12. http://logic.ti.com – Part Number Search Product Folder "Samples"
13. Logic Samples (for all Logic devices)	13. http://logic.ti.com – "How to Purchase" container "Samples"
14. Logic KnowledgeBase	14. http://logic.ti.com – "Development Support" container "Logic KBase" or http://www.ti.com/logickb
15. Logic Press Releases	15. http://logic.ti.com – "What's New" container "Press Releases"