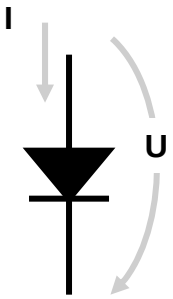
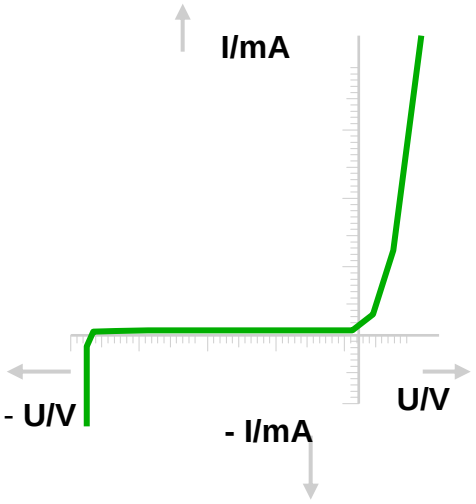
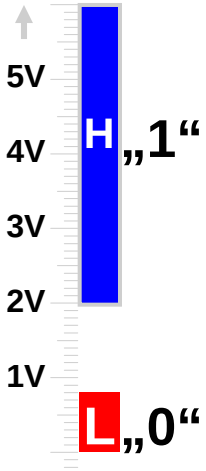
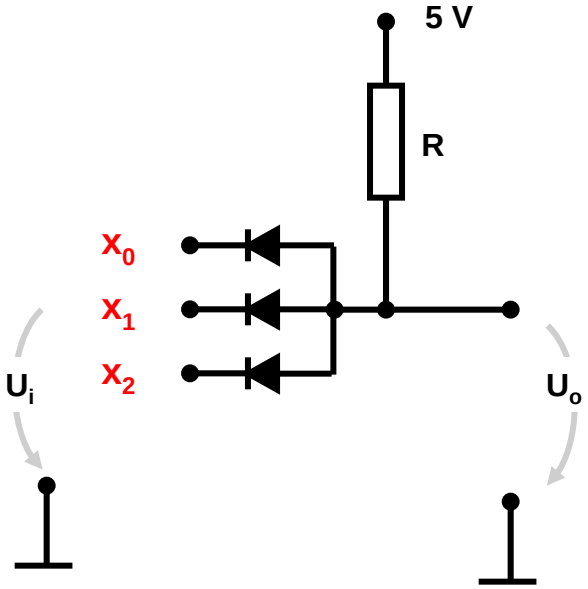
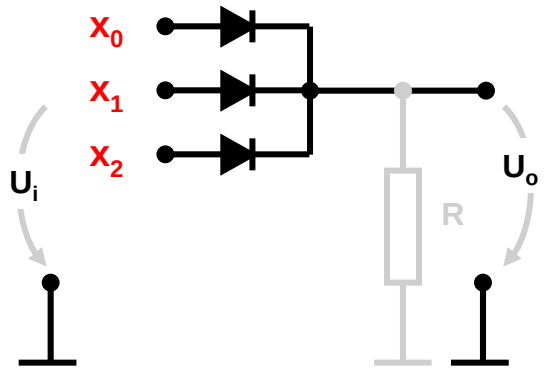
Diodenlogik



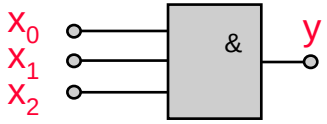




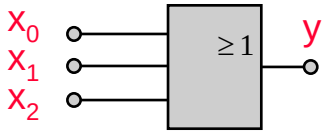




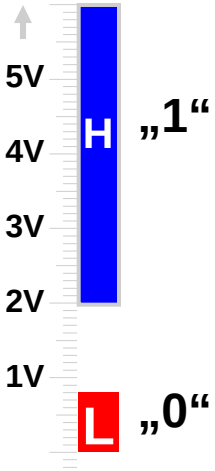
x_2	x_1	x_0	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

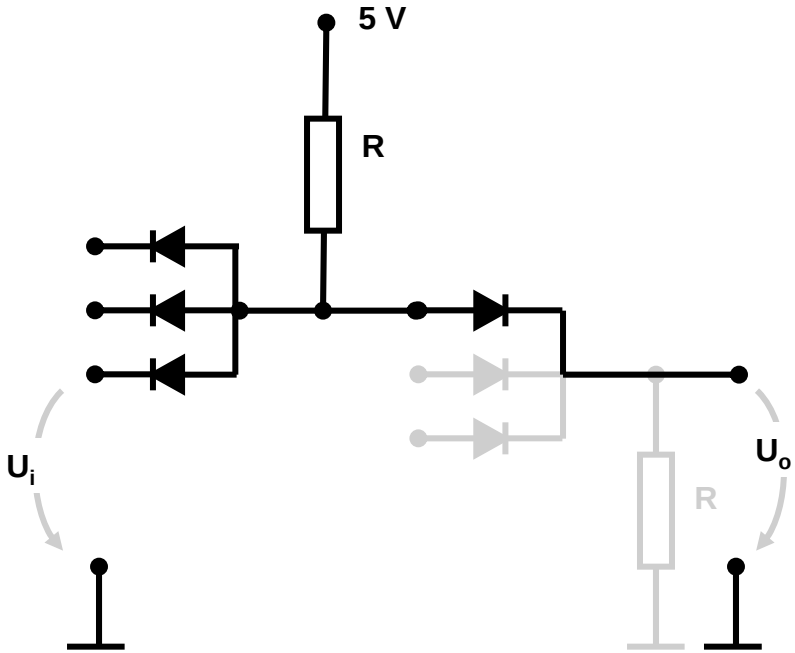


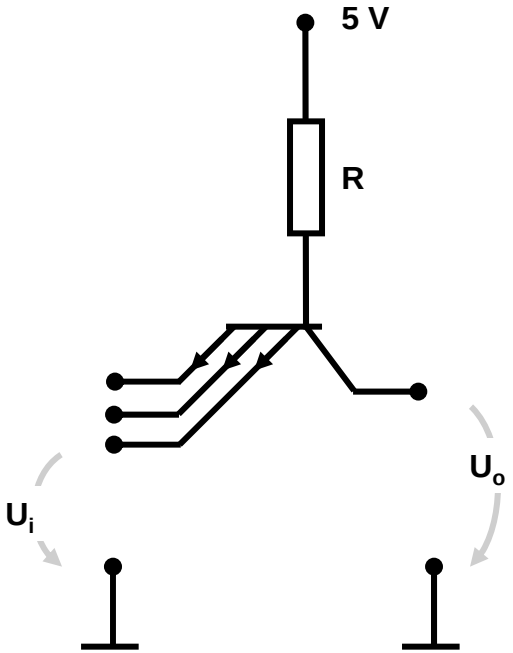
x_2	x_1	x_0	y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



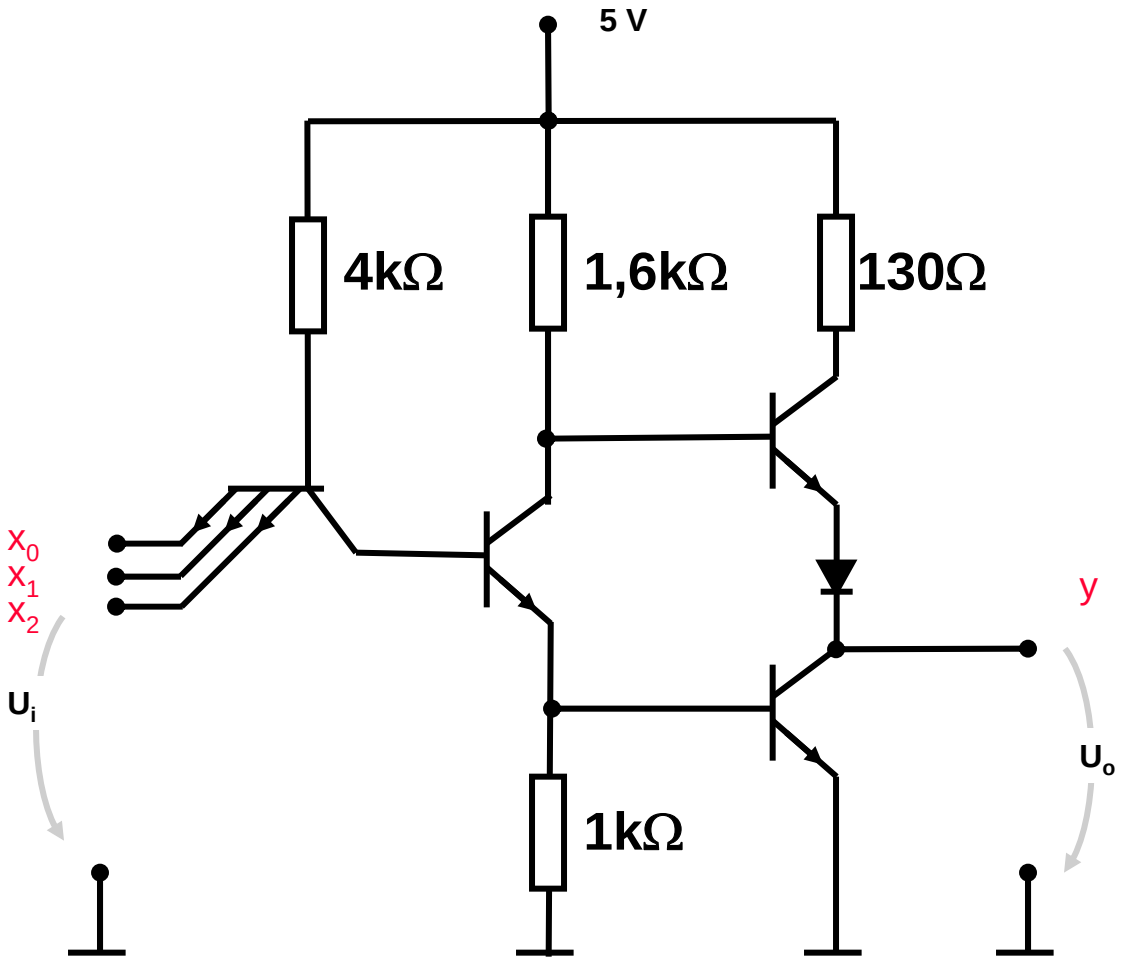
Und-Oder-Folge

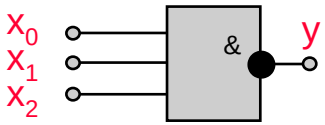






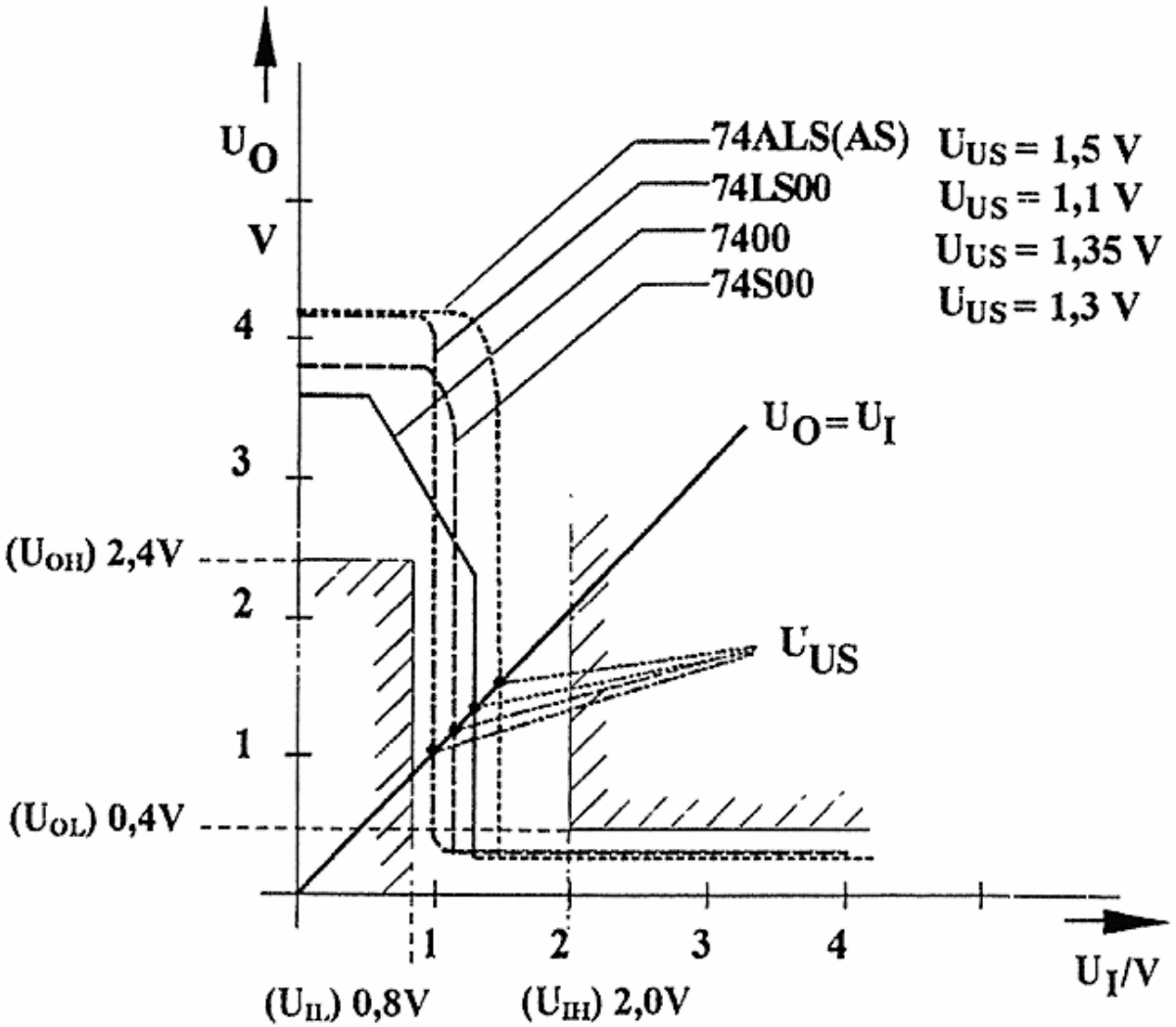
TTL- Grudgatter 7400



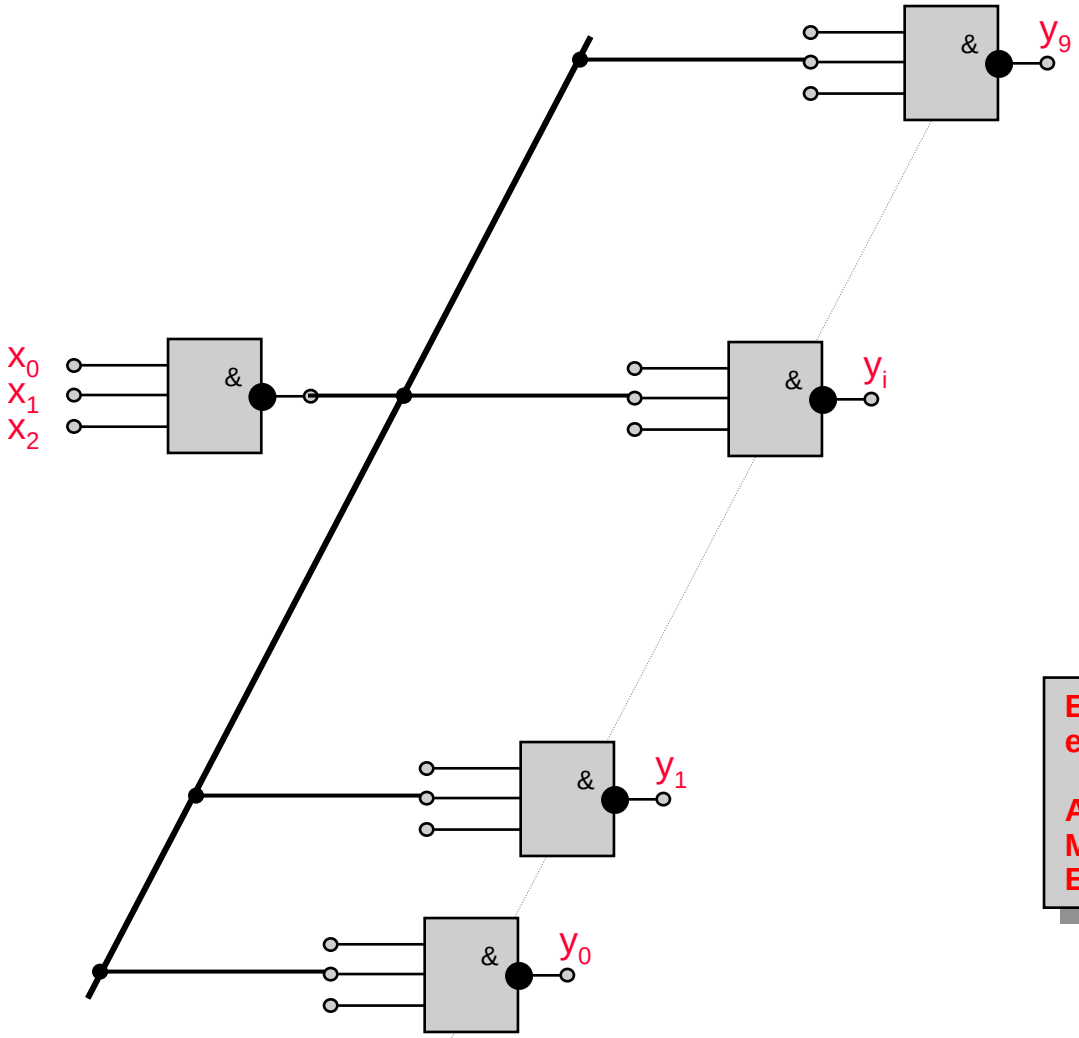


x_2	x_1	x_0	y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Transferkennlinien



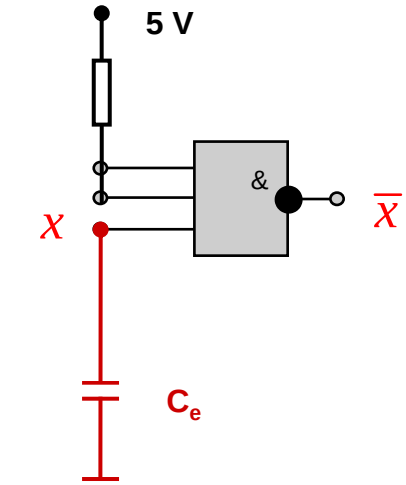
Zusammenschaltung von TTL- Gattern

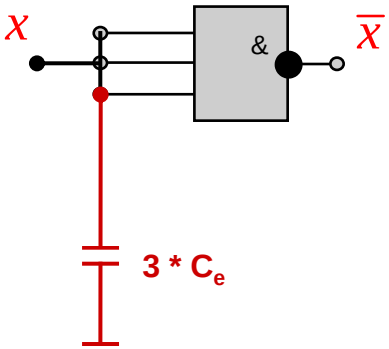


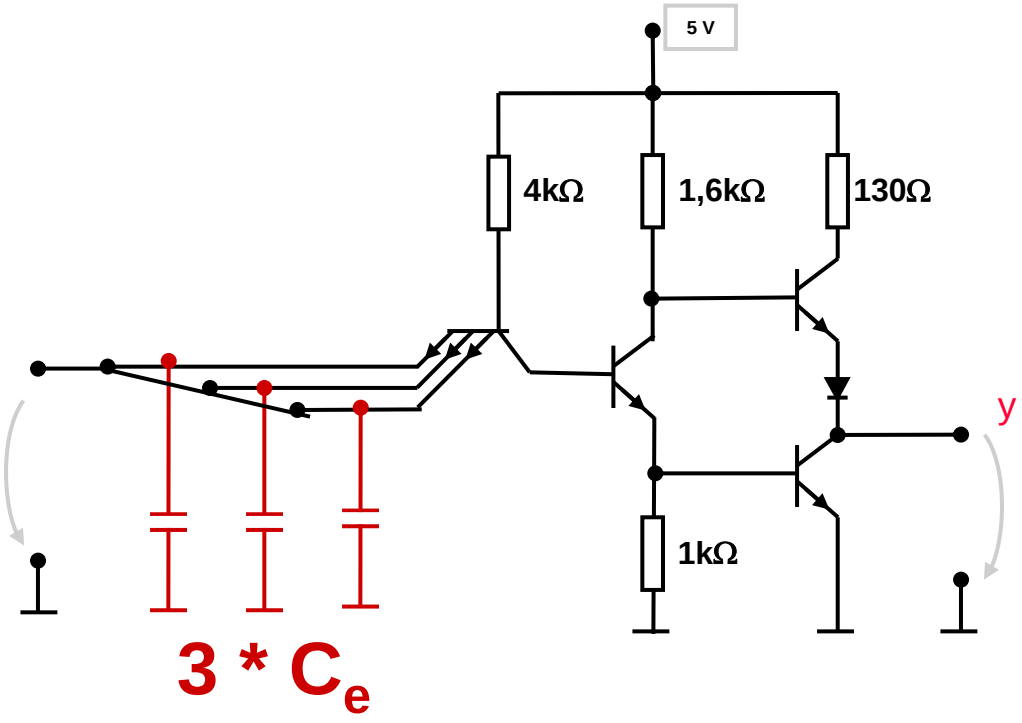
Es dürfen maximal 10 Standard-eingänge angeschlossen werden.

Achtung !
Manche Gatter haben einen erhöhten Eingangslastfaktor (2 ..).

Offene Eingänge



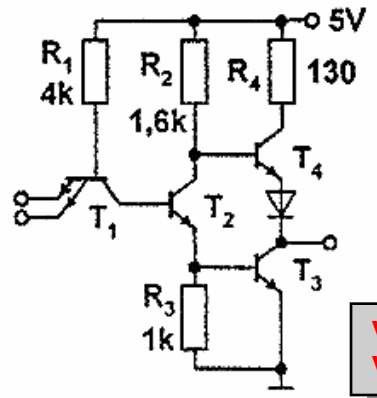




Grundgatter in TTL Technologie

7400

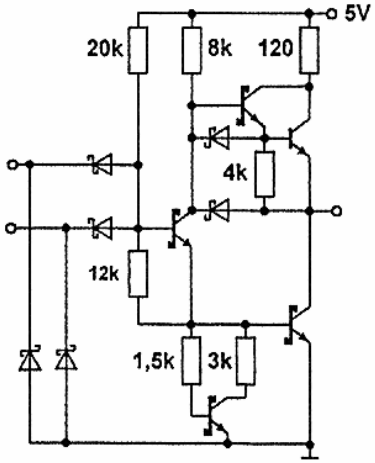
Standard-TTL



Verzögerungszeit: 10 ns
Verlustleistung: 22 mW

74LS00

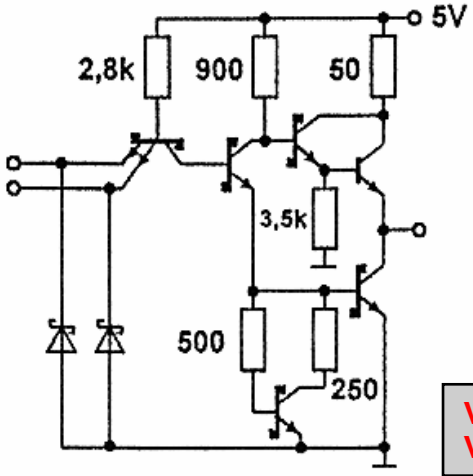
Low-power-Schottky-TTL



Verzögerungszeit: 9 ns
Verlustleistung: 2 mW

74S00

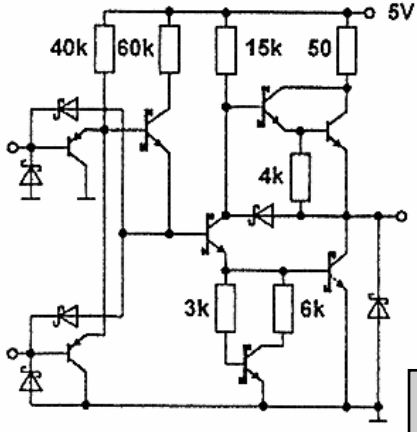
Schottky-TTL



Verzögerungszeit: 3 ns
Verlustleistung: 18 mW

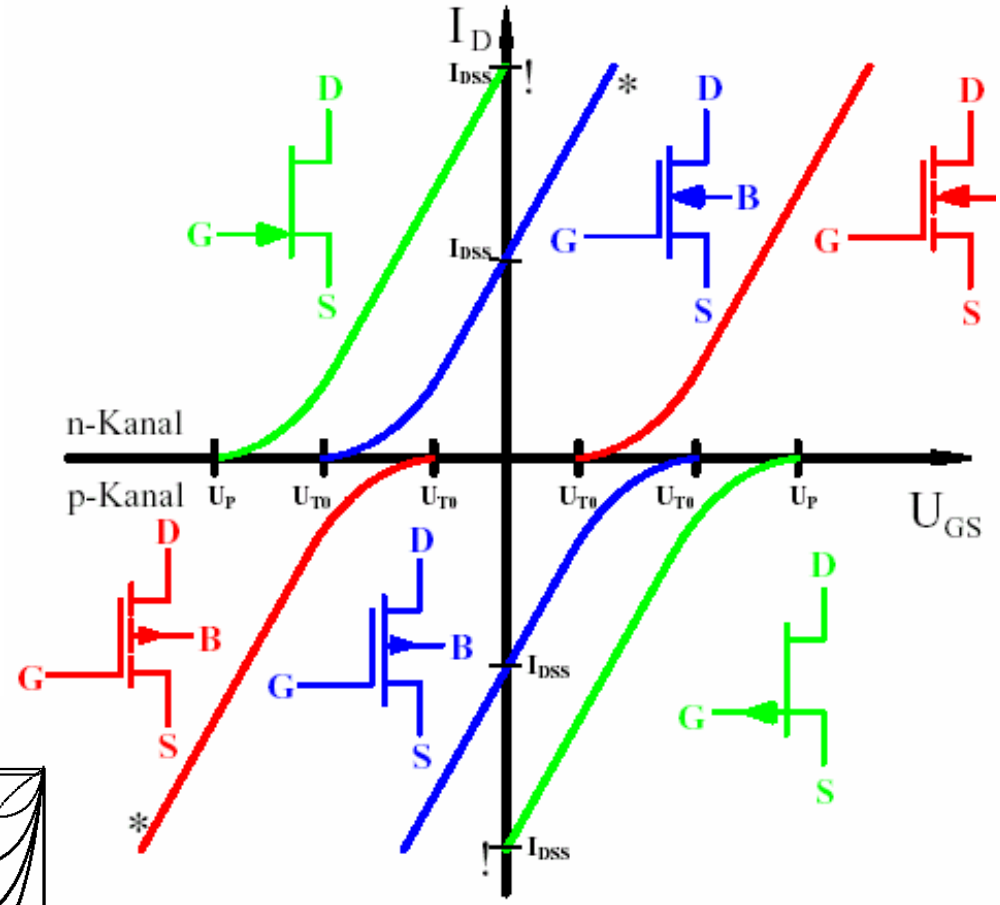
74ALS00

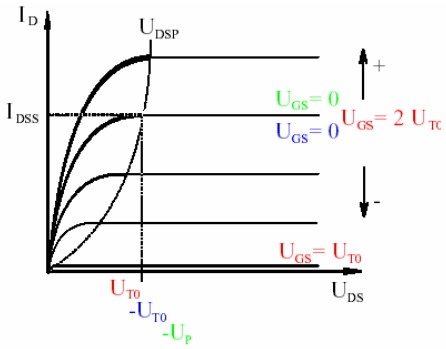
Advanced-Low-power-Schottky-TTL

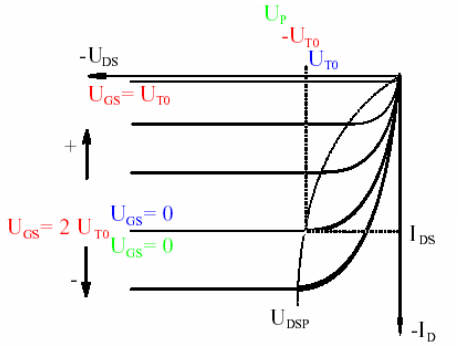


Verzögerungszeit: 4 ns
Verlustleistung: 1 mW

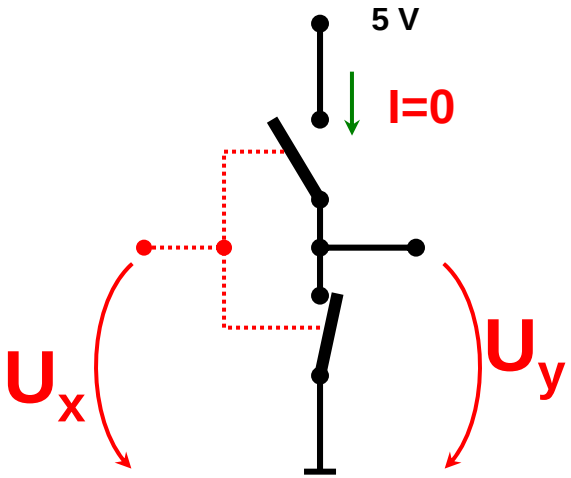
Ausgangskennlinien von MOS - Transistoren

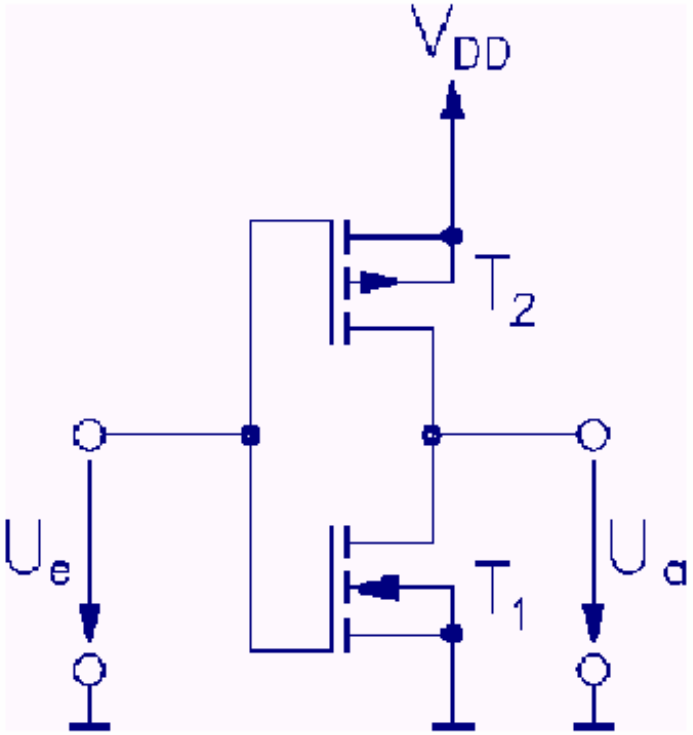




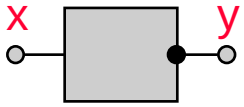


CMOS - Inverter



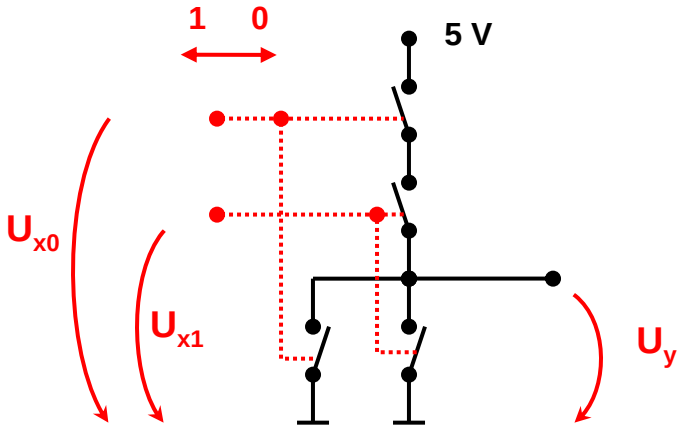


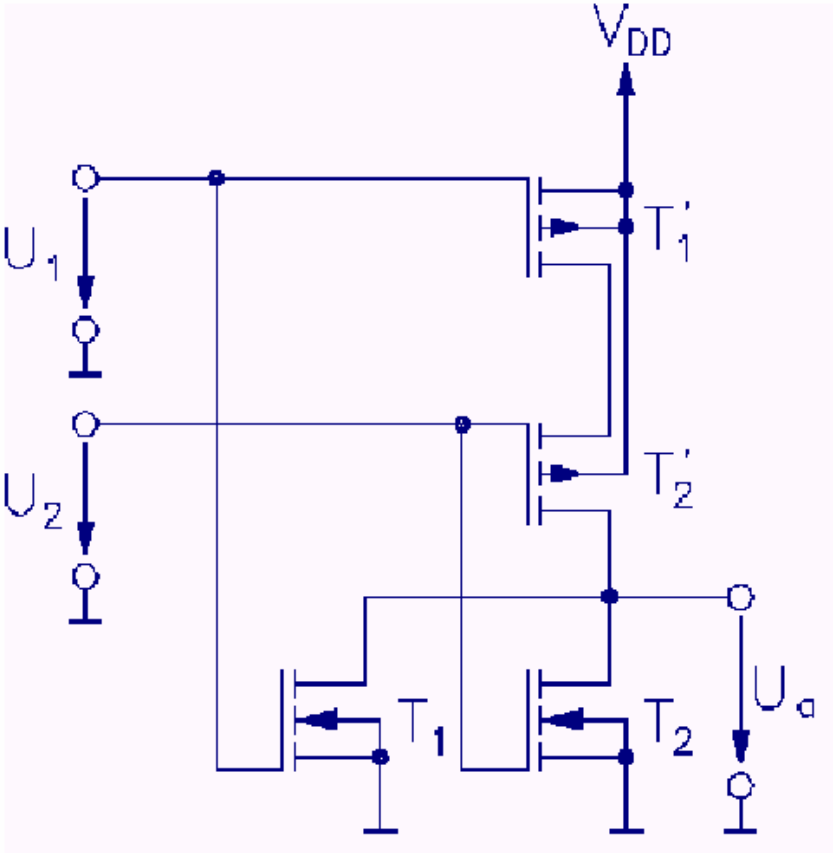
x	y
0	1
1	0

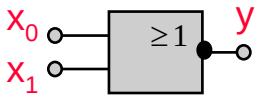


$$y = \bar{x}$$

CMOS - NOR



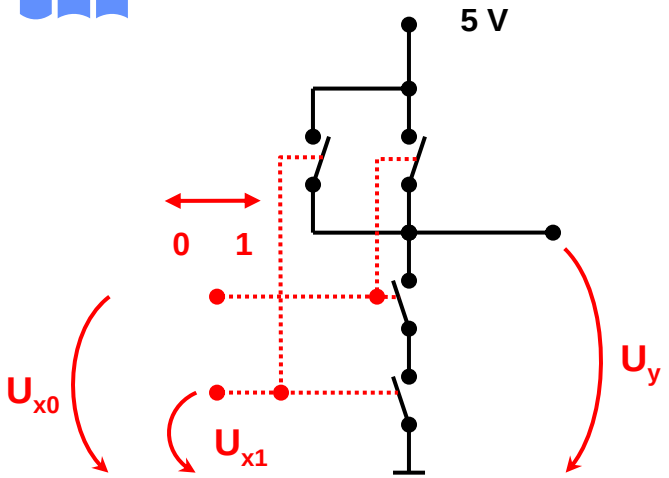




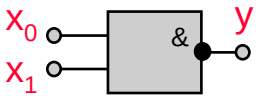
x_1	x_0	y
0	0	1
0	1	0
1	0	0
1	1	0

$$y = \overline{x_1 \vee x_0}$$
$$= \overline{x_1 + x_0}$$
$$= \overline{x_1}\ \overline{x_0}$$

CMOS - NAND



x_1	x_0	y
0	0	1
0	1	1
1	0	1
1	1	0



$$y = \overline{x_1\ x_0}$$
$$= \overline{x_1 * x_0}$$
$$= \overline{x_1 \wedge x_0}$$